STIC Search Report
EIC 2800

STIC Database Tracking Number: 127574

TO: Monica Lewis
Location:
Art Unit : 2822
Wednesday, July 21, 2004
Case Serial Number: 10/633057

From: Bode Fagbohunka
Location: EIC 2800
Jeff 4A58
Phone: 571-272-2541
bode.fagbohunka@uspto.gov

Search Notes

Examiner **Monica Lewis**

Please find attached the results of your search for **10/633057** The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka

127574

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 7/19/04 Serial # 10/633,605 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2899 Phone 272-1838 Room _____

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

7-20-04 A 8:15 IN

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___ _____

Teaching Refs ___ _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-17

Problem: See pages 1 - 2, 3 + 9 - 15 Abstract

Solution:

Staff Use Only

Searcher: Bose

Searcher Phone: 22541

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 07-20-04

Date Completed: 07-20-04

Searcher Prep/Rev Time: 40

Online Time: 240

Type of Search

Structure (#) _____

Bibliographic ✓

Litigation _____

Fulltext _____

Patent Family _____

Other _____

Vendors

STN _____

Dialog ✓

Questel/Orbit _____

Lexis-Nexis _____

WWW/Internet _____

Other _____

WHAT IS CLAIMED IS:

1. A semiconductor resistor formed in a semiconductor material of a first conductivity type, the resistor comprising:

an active region of the semiconductor material;

an isolation region formed in the semiconductor material to surround the active region, and isolate the active region from laterally adjacent regions;

a layer of insulation formed on the active region;

a semiconductor structure formed on the isolation region and the layer of insulation so that the semiconductor structure partially overlies the active region; and

a doped region of a second conductivity type formed in the active region, the doped region lying adjacent to a side wall of the semiconductor structure.

2. The semiconductor resistor of claim 1 wherein the doped region includes a first region of a first dopant concentration, a second region of a second dopant concentration, and a third region of a third dopant concentration, the first dopant concentration being substantially larger than the dopant concentrations of the second and third regions, the second and third regions lying on opposite sides of and contacting the first region.

3. The semiconductor resistor of claim 1 wherein the doped region has a length and a width, the length being substantially longer than the width.

ABSTRACT

The accuracy of the width measurement of a semiconductor resistor is improved by modifying the gate mask of a standard MOS transistor fabrication process to form an opening between regions of polysilicon that are used as a mask when the substrate or well material is implanted to form the resistor.

Day : Wednesday

PALM INTRANET

Date: 7/21/2004
Time: 08:36:42

Application Number Information

Application Number: **10/633057**
Assignments
Filing Date: **08/01/2003**
Effective Date: **08/01/2003**
Application Received: **08/04/2003**
Patent Number:
Issue Date: **00/00/0000**
Date of Abandonment: **00/00/0000**
Attorney Docket Number: **100-22300**
Status: **30 /DOCKETED NEW CASE - READY FOR EXAMINATION**
Confirmation Number: **3600**

Examiner Number: **73172 / LEWIS, MONICA**
Group Art Unit: **2822** **IFW IMAGE**
Class/Subclass: **257/542.000**
Lost Case: **NO**
Interference Number:
Unmatched Petition: **NO**
L&R Code: Secrecy Code:**1**
Third Level Review: **NO** Secrecy Order: **NO**
Status Date: **04/26/2004**
Oral Hearing: **NO**

Title of Invention: **SEMICONDUCTOR RESISTOR AND METHOD OF FORMING THE RESISTOR THAT IMPROVES THE ACCURACY OF THE WIDTH MEASUREMENT**

Bar Code | PALM Location | Location Date | Charge to Loc | Charge to Name | Employee Name | Location

Appln Info | Contents | Petition Info | Atty/Agent Info | Continuity Data | Foreign Data

Search Another: Application# [ ] Search **or Patent#** [ ] Search

PCT / [ ] / [ ] Search **or PG PUBS #** [ ] Search

Attorney Docket # [ ] Search

Bar Code # [ ] Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

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Set     Items   Description
S1       1944   AU=(TAYLOR R? OR TAYLOR, R?)
S2         45   S1 AND (SEMI()CONDUCT? OR SEMICONDUCT?)
S3         12   S2 AND RESISTOR?
S4         12   IDPAT (sorted in duplicate/non-duplicate order)
S5         11   IDPAT (primary/non-duplicate records only)
S6     132980   DOPED OR DOPING OR DOPE
S7         21   S6 AND S1
S8         11   S7 AND RESIST?
S9          8   S8 NOT S5
?  show files
File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Jul W02
         (c) 2004 European Patent Office
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200445
         (c) 2004  Thomson Derwent
File 349:PCT Fulltext 1979-2002/UB=20040708,UT=20040701
         (c) 2004 WIPO/Univentio
?
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9/TI,PN,PD,AN,AD,AB,K/5 (Item 5 from file: 348)

Method and resulting devices for compensating for process variables in a CMOS device driver circuit.
Verfahren und daraus resultierende Vorrichtungen zur Kompensation von Prozessparametern in einer CMOS-Treiberschaltung.
Procede et dispositifs obtenus pour compenser les parametres du processus dans un circuit de commande de type CMOS.

PATENT (CC, No, Kind, Date): EP 410123 A2 910130 (Basic)
EP 410123 A3 920923
APPLICATION (CC, No, Date): EP 90110958 900609;
PRIORITY (CC, No, Date): US 385629 890726

ABSTRACT EP 410123 A2

According to the present invention, an improved CMOS integrated circuit and an improved method of forming the circuit is provided. The circuit has a first FET device (26; 38) and a second FET device (60; 72), and at least one performance characteristic of said first and second FET devices varies in the same manner with the variation of at least one performance related process variable condition. Each of said FET devices has an output signal at least one characteristic of which is changed by a change in the performance related variable condition. The first and second FET devices are connected such that the one output characteristic of the second FET device acts in opposition to the one output characteristic of the first FET device to provide a merged output signal representative of the combined effect of the two FET devices. The second FET device is constructed so as to be more responsive to the variations in said performance related variable condition than the first FET device and to have a weaker output signal than the first FET device, whereby the merged output signal of the two FET devices is maintained relatively constant irrespective of variations in the performance related variable condition. (see image in original document)

INVENTOR:
... US)
Taylor, Robert Simpson ...

...SPECIFICATION turn-on time for each successive finger is delayed by a time proportionate to the **resistance** of the gate and its capacitance. Since gate **resistance** increases as channel length decreases, this technique reduces the delay variation with channel length variation...

...with certain types of silicides, an extra mask may be required to generate a precision **resistor** when this technique is used.
Another technique for reducing the effect of processing variables is... dielectric between the gate electrode and the channel, the base mobility dictated by the background **doping** level, variations in channel width (this is a small effect but not completely negligible); and...
?

```
Set     Items   Description
S1   14186712   WIDTH OR BREADTH OR THICKNESS OR SIZE OR SIZES OR MEASUREM-
             ENT? OR DIMENSION?
S2    3091810   RESISTOR OR RESISTANCE
S3     886178   GATE?
S4     420908   MASK?
S5    4505384   MOS? ? OR MOSFET? ? OR FET? ? OR METAL()OXIDE()SEMICONDUCT-
             OR? OR FIELD()EFFECT?()TRANSIST? OR PMOS OR CMOS
S6     789425   DOPED OR DOPING OR DOPE
S7   12265838   REGION? OR SECTION? OR SEGMENT? OR AREA?
S8      30971   S6(6N)S7
S9       1530   (S1 OR LENGTH?) AND S2 AND S8
S10        43   (S1 OR LENGTH?) (3N) S2 (3N)S8
S11        21   S10 AND (S3 OR S4 OR S5)
S12        14   RD (unique items)
S13        86   S9 AND S3 AND S4 AND S5
S14        85   S13 NOT S12
S15        85   RD (unique items)
S16         1   S15 AND PD<=20030804
S17        82   S15 AND PY<=2003
S18       111   (S1 OR LENGTH?) (6N) S2 (6N)S8
S19         3   S18 AND S3 AND S4 AND S5
S20         3   S19 NOT S16
S21         2   S20 NOT S12
? show files
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         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
File  94:JICST-EPlus 1985-2004/Jun W4
         (c)2004 Japan Science and Tech Corp(JST)
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File 144:Pascal 1973-2004/Jul W2
         (c) 2004 INIST/CNRS
File 647:CMP  Computer Fulltext 1988-2004/Jul W2
         (c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Jul 20
         (c) 2004 The Dialog Corp.
File  35:Dissertation Abs Online 1861-2004/May
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         (c) 2004  Thomson Derwent
File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)
         (c) 2004 JPO & JAPIO
File 202:Info. Sci. & Tech. Abs. 1966-2004/Jul 12
         (c) 2004 EBSCO Publishing
File 239:Mathsci 1940-2004/Sep
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Set     Items   Description
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             ENT? OR DIMENSION?
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S3     886178   GATE?
S4     420908   MASK?
S5    4505384   MOS? ? OR MOSFET? ? OR FET? ? OR METAL()OXIDE()SEMICONDUCT-
             OR? OR FIELD()EFFECT?()TRANSIST? OR PMOS OR CMOS
S6     789425   DOPED OR DOPING OR DOPE
S7   12265838   REGION? OR SECTION? OR SEGMENT? OR AREA?
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S11        21   S10 AND (S3 OR S4 OR S5)
S12        14   RD (unique items)
S13        86   S9 AND S3 AND S4 AND S5
S14        85   S13 NOT S12
S15        85   RD (unique items)
S16         1   S15 AND PD<=20030804
S17        82   S15 AND PY<=2003
S18       111   (S1 OR LENGTH?) (6N) S2 (6N)S8
S19         3   S18 AND S3 AND S4 AND S5
S20         3   S19 NOT S16
S21         2   S20 NOT S12
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File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W2
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
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         (c) 2004 The HW Wilson Co.
File  94:JICST-EPlus 1985-2004/Jun W4
         (c)2004 Japan Science and Tech Corp(JST)
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File 202:Info. Sci. & Tech. Abs. 1966-2004/Jul 12
         (c) 2004 EBSCO Publishing
File 239:Mathsci 1940-2004/Sep
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File 25:Weldasearch 1966-2003/Dec

File 62:SPIN(R) 1975-2004/May W4

File 96:FLUIDEX 1972-2004/Jul

File 98:General Sci Abs/Full-Text 1984-2004/Jun

File 266:FEDRIP 2004/May

?

12/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7758604 INSPEC Abstract Number: B2003-11-2560R-079
Title: Influence of depletion region length on specific on-resistance in SiC MOSFET
Author(s): Ohtsuka, K.; Tarui, Y.; Imaizumi, M.; Sugimoto, H.; Takami, T.; Ozeki, T.
Author Affiliation: Mitsubishi Electr. Corp., Hyogo, Japan
Journal: Materials Science Forum Conference Title: Mater. Sci. Forum (Switzerland) vol.433-436 p.765-8
Publisher: Trans Tech Publications,
Publication Date: 2003 Country of Publication: Switzerland
CODEN: MSFOEP ISSN: 0255-5476
SICI: 0255-5476(2003)433/436L.765:IDRL;1-5
Material Identity Number: H866-2003-012
Conference Title: Silicon Carbide and Related Materials 2002. ECSCRM 2002. 4th European Conference on Silicon Carbide and Related Materials
Conference Sponsor: Eur. Commission High-Level Sci. Conferences Contract No. HPCF - CT - 1999 - 00181; Vetenskapsradet Swedish Res. Council; et al
Conference Date: 2-5 Sept. 2002 Conference Location: Linkoping, Sweden
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Practical (P); Theoretical (T); Experimental (X)
Abstract: SiC **metal - oxide - semiconductor field effect transistor** (**MOSFET**) with n-layer channel structure is fabricated and characterized. Influence of depletion region **length** on specific on-**resistance** is investigated from calculation and experiment. Depletion **region length** over 5 mu m or **doping** of drift layer over 5*10/sup 15//cm/sup 3/ are required for depletion region resistance below 10 m Omega cm/sup 2/ from the calculation. The evaluated values are coincident with the values measured from fabricated SiC **MOSFETs** epilayer channel **MOSFET** and channel doped **MOSFET** . (6 Refs)
Subfile: B
Descriptors: **MOSFET** ; semiconductor device models; semiconductor epitaxial layers; semiconductor growth; silicon compounds; wide band gap semiconductors
Identifiers: depletion region length influence; SiC **metal oxide semiconductor field effect transistor** ; resistance; SiC **MOSFET** fabrication; drift layer doping; epilayer channel **MOSFET** ; channel doped **MOSFET** ; 5 micron; SiC
Class Codes: B2560R (Insulated gate field effect transistors); B2520M (Other semiconductor materials); B2550B (Semiconductor doping); B2560B (Semiconductor device modelling and equivalent circuits)
Chemical Indexing:
SiC int - Si int - C int - SiC bin - Si bin - C bin (Elements - 2)
Numerical Indexing: size 5.0E-06 m

12/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4654413 INSPEC Abstract Number: B9406-2560R-012
Title: Device simulation of a thin-film silicon on insulator power metal - oxide - semiconductor field - effect transistor **for structure optimization**
Author(s): Matsumoto, S.; Yoshino, H.

Author Affiliation: NTT Interdisciplinary Res. Labs., Tokyo, Japan
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers & Short Notes) vol.33, no.1B p.519-23
Publication Date: Jan. 1994 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
Conference Title: 1993 International Conference on Solid State Devices and Materials (SSDM '93)
Conference Sponsor: Japan Soc. Appl. Phys
Conference Date: 29 Aug.-1 Sept. 1993 Conference Location: Chiba, Japan
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The authors propose an optimised device structure based on the results of numerically simulating thin-film silicon on insulator (SOI) power **metal - oxide - semiconductor field - effect transistors** (**MOSFETs**) in the 50-V class. The dependence of the breakdown voltage and specific on- **resistance** on the **doping** concentration of the drain offset **region** , on the **thickness** of the superficial silicon layer, on the thickness of the buried oxide layer, and on the drain offset length are compared for buried channel **MOSFETs** and surface channel **MOSFETs** . (9 Refs)
Subfile: B
Descriptors: electric breakdown of solids; elemental semiconductors; insulated **gate field effect transistors** ; power transistors; semiconductor device models; semiconductor-insulator boundaries; silicon
Identifiers: SOI power **MOSFET** ; VLSI; **CMOS** ; device simulation; thin film SOI; elemental semiconductor; structure optimization; optimised device structure; breakdown voltage; specific on-resistance; doping concentration; drain offset region; thickness; buried oxide layer; drain offset length; buried channel; surface channel; 50 V; Si-SiO/sub 2
Class Codes: B2560R (Insulated gate field effect transistors); B2560B (Modelling and equivalent circuits)
Chemical Indexing:
Si-SiO2 int - SiO2 int - O2 int - Si int - O int - SiO2 bin - O2 bin - Si bin - O bin - Si el (Elements - 1,2,2)
Numerical Indexing: voltage 5.0E+01 V

12/9/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014088150 **Image available**
WPI Acc No: 2001-572364/200165
XRPX Acc No: N01-426649
Power semiconductor device with integral source-emitter ballast resistor, has resistor regions of N-type dopants and highly doped contact regions to provide ohmic metal contact to emitter resistor regions
Patent Assignee: INTERSIL CORP (INTE-N); FAIRCHILD SEMICONDUCTOR CORP (FAIH)
Inventor: BHALLA A; MURALEEDHARAN SHENOY P
Number of Countries: 028 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1104027	A2	20010530	EP 2000121970	A	20001009	200165	B
JP 2001189455	A	20010710	JP 2000360784	A	20001128	200165	
KR 2001051995	A	20010625	KR 200071297	A	20001128	200172	
US 6437419	B1	20020820	US 99450872	A	19991129	200257	

Priority Applications (No Type Date): US 99450872 A 19991129
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1104027	A2	E	19	H01L-029/08	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2001189455	A		16	H01L-029/78	
KR 2001051995	A			H01L-021/328	
US 6437419	B1			H01L-027/082	

Abstract (Basic): EP 1104027 A2

NOVELTY - Source or emitter region is provided in P-well (30) of semiconductor device with two lightly **doped resistor regions** of N-type dopants, extending along **length** of P-well and beneath sidewall spacer insulator (19) of **gate** (16). Highly doped N-type contact regions (40) in substrate (12), extend transverse to edges of partial **gate** structures, to provide ohmic metal contact to elongated emitter resistor regions.

DETAILED DESCRIPTION - The regions of the substrate between the **gate** sidewall spacer insulators and between heavily doped N-type regions are heavily doped with P-type dopants. In these regions, N-type dopants are substituted for P-type dopants and viceversa, including one of group consisting of **MOSFET** , IGBT, MCT and DMOS devices. The partial **gate** structures are either stripes or cells. The resistors (20) alter the normal threshold voltage by a few millivolts and short circuit threshold voltage by more than 10%. An INDEPENDENT CLAIM is also included for method of forming semiconductor device with integral source-emitter ballast resistor.

USE - Power semiconductor devices such as IGBT, DMOS, **MOSFET** and MCT.

ADVANTAGE - The device has negligible effect at operating current and adjusts the threshold voltage under short circuit conditions. Emitter resistors protect the device carrying excess current during short circuit conditions.

DESCRIPTION OF DRAWING(S) - The figure shows the partial perspective view of semiconductor structure with self-aligned ballast emitter source resistors.

Substrate (12)
Gate (16)
Sidewall spacer insulator (19)
Resistor (20)
P-well (30)
N-type contact regions (40)
pp; 19 DwgNo 1a/12

Title Terms: POWER; SEMICONDUCTOR; DEVICE; INTEGRAL; SOURCE; EMITTER; BALLAST; RESISTOR; RESISTOR; REGION; N; TYPE; DOPE; HIGH; DOPE; CONTACT; REGION; OHM; METAL; CONTACT; EMITTER; RESISTOR; REGION
Derwent Class: U11; U12
International Patent Class (Main): H01L-021/328; H01L-027/082; H01L-029/08; H01L-029/78
International Patent Class (Additional): H01L-021/331; H01L-021/332; H01L-021/336; H01L-029/739; H01L-029/745; H01L-029/749
File Segment: EPI
Manual Codes (EPI/S-X): U11-C18A2; U11-C18A3; U11-C18B2; U12-D01B1; U12-D02A

12/9/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013258271 **Image available**
WPI Acc No: 2000-430154/200037
XRAM Acc No: C00-130650
XRPX Acc No: N00-320917

Transistor used as an active component of an integrated circuit, comprises lightly doped drain and source/drain areas, which are formed simultaneously for high performance transistors

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: GARDNER M I

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6069387	A	20000530	US 9855648	A	19980406	200037	B

Priority Applications (No Type Date): US 9855648 A 19980406
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6069387	A		8	H01L-029/76	

Abstract (Basic): US 6069387 A

NOVELTY - A transistor comprises an etch-stop layer formed across a semiconductor substrate (100), a high-K **gate** dielectric, and a **gate** conductor (110). Lightly doped drain (124) and source/drain regions (122) are self-aligned with sidewall surfaces of the **gate** dielectric and **gate** conductor, respectively.

USE - For use as an active component of an integrated circuit.

ADVANTAGE - The invention eliminates the need for sidewall spacers to facilitate fabrication of sub-micron **gate** conductors and allow increased control of lightly doped drain **dimensions** , thus minimizing parasitic **resistance** in transistors having small lateral **dimensions** . Lightly **doped** drain **areas** are fabricated simultaneously with source/drain areas, thus simplifying the manufacturing process and improving device quality.

DESCRIPTION OF DRAWING(S) - The figure shows a partial cross-sectional view of a semiconductor topography.

Semiconductor substrate (100)
Gate conductor (110)
Source/drain regions (122)
Lightly doped drain regions (124)
Metal silicide (128)
pp; 8 DwgNo 9/9

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The etch-stop layer comprises a layer of silicon nitride. The **gate** dielectric comprises tantalum oxide, cerium oxide, tin oxide, barium strontium titanate, lead lanthanum zirconate titanate, or barium zirconate titanate. The transistor further comprises metal silicide (128) formed on upper surfaces of the **gate** conductor and the source/drain areas. The **gate** conductor comprises polysilicon.

Preferred Properties: The silicon nitride layer has a thickness of 5-10 Angstrom. The **gate** dielectric has a lateral thickness of 60-80 % of the lateral thickness of the **gate** conductor. It has a dielectric constant greater than 3.8.

Title Terms: TRANSISTOR; ACTIVE; COMPONENT; INTEGRATE; CIRCUIT; COMPRISE; LIGHT; DOPE; DRAIN; SOURCE; DRAIN; AREA; FORMING; SIMULTANEOUS; HIGH; PERFORMANCE; TRANSISTOR
Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-029/76
International Patent Class (Additional): H01L-029/94

File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C10B; L04-C10F; L04-C12A; L04-C12B; L04-E01
Manual Codes (EPI/S-X): U11-C02J6; U11-C05E3; U11-C05F1; U12-D02A3; U12-Q
Derwent Registry Numbers: 1506-U; 1531-U

12/9/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012651045 **Image available**
WPI Acc No: 1999-457150/199938
XRAM Acc No: C99-134154
XRPX Acc No: N99-341854
Test device for determining resistance of components in metal oxide semiconductor field effect transistors **including total parasitic resistance**
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: BOTHRA S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5933020	A	19990803	US 96731528	A	19961016	199938	B

Priority Applications (No Type Date): US 96731528 A 19961016
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5933020	A		14	G01R-031/22	

Abstract (Basic): US 5933020 A

NOVELTY - The semiconductor device is constructed with a set of contacts made to a set of silicided regions in a semiconductor substrate (502), a second set of contacts are made to a second set of silicide regions separated by channel regions (510) and **gates** (512) of a transistor. By comparing the resistance values between the contacts in the two sets, one through silicide alone and the other through silicide and the channel and the lightly doped drain **measurements** of silicide sheet **resistance** , **resistance** of the lightly **doped regions** and parasitic **resistance** can be determined.

DETAILED DESCRIPTION - Test structure for determining the parasitic resistance of a semiconductor device comprising:

(a) first test device for determining contact resistance between contacts and a silicided region and sheet resistance of the silicided region comprising: first silicided region with a passivation layer over it, and a number of first contacts formed through the passivation layer to contact the silicided region which are separated from each other by varying distances and electrically coupled together via the silicided region;

(b) second test device comprising: a number of second silicided regions with a number of channel regions of varying length disposed between the silicided regions and each peripherally surrounded by a lightly doped region; number of **gates** of varying length overlying the channel regions; second passivation layer over the second silicided regions, and a number of contacts separated by varying distances formed through it to contact the second silicided regions. The second test device is for determining total resistance between any two of the second contacts, and the first and second devices are related such that dominant parasitic resistance components of the semiconductor device are determined by comparing measurements taken using the two devices.

USE - **Metal oxide semiconductor field effect transistors**

MOSFETs .

ADVANTAGE - The resistance of the various components of the device can be determined and its total parasitic resistance and the effect on device performance determined.

DESCRIPTION OF DRAWING(S) - The drawing shows a test structure.

Semiconductor substrate (502)

Wells (504)

Silicided regions (506)

Lightly doped regions (508)

Channel regions (510)

Gates (512)

Contacts (516)

pp; 14 DwgNo 5A/8

Title Terms: TEST; DEVICE; DETERMINE; RESISTANCE; COMPONENT; METAL; OXIDE; SEMICONDUCTOR; FIELD; EFFECT; TRANSISTOR; TOTAL; PARASITIC; RESISTANCE

Derwent Class: L03; S01; U11

International Patent Class (Main): G01R-031/22

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C10F; L04-C13B; L04-C18; L04-E01B1

Manual Codes (EPI/S-X): S01-D05B1; S01-G02B; U11-F01C1; U11-F01C5

12/9/6 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010662855 **Image available**

WPI Acc No: 1996-159809/199616

XRPX Acc No: N96-133911

Field effect transistor with improved ESD protection - has drain region with lightly doped ballast resistor extending across width of drain and separating two other drain sub-regions and ballast resistor laterally distributes current along width of drain during ESD pulse

Patent Assignee: NCR INT INC (NATC); NCR CORP (NATC)

Inventor: GIOIA S C; WALKER J D

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5498892	A	19960312	US 93129231	A	19930929	199616	B
JP 7153945	A	19950616	JP 94224384	A	19940920	199616	

Priority Applications (No Type Date): US 93129231 A 19930929

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5498892	A		15	H01L-029/68	
JP 7153945	A		9	H01L-029/78	

Abstract (Basic): US 5498892 A

The **field effect transistor** comprises a source region and channel region with opposite dopant type to source region underlying a **gate** electrode. A drain region is separated from the source region by the channel region. The drain region includes a ballast region separating two other drain sub-regions.

One drain sub-region is located between the ballast region and the channel. The other drain sub-region is connected to a device exterior to the transistor. The ballast region has a resistance greater than that of the drain regions thereby laterally distributing current flowing between the channel region and signal connection points.

USE/ADVANTAGE - For very large scale integrated circuits made with **MOSFET** 's. Ballast reduces peak current densities and thus limits damage and failures.

Dwg.1/12
Title Terms: FIELD; EFFECT; TRANSISTOR; IMPROVE; ESD; PROTECT; DRAIN; REGION; LIGHT; DOPE; BALLAST; RESISTOR; EXTEND; WIDTH; DRAIN; SEPARATE; TWO; DRAIN; SUB; REGION; BALLAST; RESISTOR; LATERAL; DISTRIBUTE; CURRENT; WIDTH; DRAIN; ESD; PULSE
Derwent Class: U11; U12; U13
International Patent Class (Main): H01L-029/68; H01L-029/78
International Patent Class (Additional): H01L-021/265
File Segment: EPI
Manual Codes (EPI/S-X): U11-C02J6; U12-D02A3; U13-E01

12/9/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010199465 **Image available**
WPI Acc No: 1995-100719/199514
XRPX Acc No: N95-079659
Integrated circuit with FET source-drain coupled through resistor to conductor - has resistor formed in doped tub region connected by heavily doped contact to output conductor, with resistor size defined by masking conductor formed in gate conductor layer
Patent Assignee: AT & T CORP (AMTT); AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: SMOOHA Y
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2281813	A	19950315	GB 9417498	A	19940831	199514	B
JP 7183516	A	19950721	JP 94238605	A	19940907	199538	
GB 2281813	B	19970416	GB 9417498	A	19940831	199719	
US 5838033	A	19981117	US 93118109	A	19930908	199902	
KR 204986	B1	19990615	KR 9422412	A	19940907	200063	

Priority Applications (No Type Date): US 93118109 A 19930908
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2281813	A		14	H01L-027/04	
JP 7183516	A		6	H01L-029/78	
GB 2281813	B			H01L-027/04	
US 5838033	A			H01L-029/76	
KR 204986	B1			H01L-027/04	

Abstract (Basic): GB 2281813 A

The IC includes a **FET** with a **gate** conductor (406) formed from a layer over a semiconductor substrate (400). The resistor is formed in a well region (401) connected to a circuit conductor (410) through a heavily doped contact region (402) in the tub. The tub and contact region are the same conductivity type as the **FET** source-drain region. The **FET** source-drain region is also connected to the circuit conductor.

The resistor underlies a resistor **masking** conductor (408) formed from the conductor layer, so that the resistor **mask** defines the resistor size. Pref. the resistor **masking** conductor is connected (409) to the circuit conductor, which may be an output conductor connected to a bond pad.

USE/ADVANTAGE - ESD protection; output buffer. Min. lithographic feature size for resistor length; reduced buffer size; avoids extra process steps e.g. for LDD.

Dwg.4/6
Abstract (Equivalent): GB 2281813 B
An integrated circuit including a **field effect transistor** having a **gate** conductor formed from a conductor layer overlying a semiconductor body , and having a source/drain region of a given conductivity type that is coupled to a circuit conductor through a resistor, characterised in that said resistor is formed in a tub region of said given conductivity type, with said tube region being connected to said circuit conductor by means of a heavily doped contact region of said given conductivity type that is formed in said tub region; and wherein said resistor underlies a resistor **masking** conductor formed from said conductor layer, whereby the size of said resistor is defined by said resistor **masking** conductor.
Dwg.0/0
Title Terms: INTEGRATE; CIRCUIT; **FET** ; SOURCE; DRAIN; COUPLE; THROUGH; RESISTOR; CONDUCTOR; RESISTOR; FORMING; DOPE; TUB; REGION; CONNECT; HEAVY ; DOPE; CONTACT; OUTPUT; CONDUCTOR; RESISTOR; SIZE; DEFINE; **MASK** ; CONDUCTOR; FORMING; **GATE** ; CONDUCTOR; LAYER
Derwent Class: U13
International Patent Class (Main): H01L-027/04; H01L-029/76; H01L-029/78
International Patent Class (Additional): H01L-021/8238; H01L-027/092
File Segment: EPI
Manual Codes (EPI/S-X): U13-D03A; U13-E01; U13-E09

12/9/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008661959 **Image available**
WPI Acc No: 1991-165986/199123
XRPX Acc No: N91-127267
Matrix addressable display forming method - providing resistance element in each transistor circuit for limiting effect of short-circuit which may occur in transistor
Patent Assignee: GENERAL ELECTRIC CO PLC (ENGE)
Inventor: HAWS S A; LOWE A J; RUNDLE P C; TOMES D W
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 430487	A	19910605	EP 90312404	A	19901114	199123	B
GB 2238644	A	19910605	GB 8926760	A	19891129	199123	
JP 3198380	A	19910829	JP 90325130	A	19901127	199141	
EP 430487	A3	19920429	EP 90312404	A	19901114	199329	
US 5278086	A	19940111	US 90618651	A	19901127	199403	
GB 2238644	B	19940202	GB 8926960	A	19891129	199404	
EP 430487	B1	19950517	EP 90312404	A	19901114	199524	
DE 69019475	E	19950622	DE 619475	A	19901114	199530	
			EP 90312404	A	19901114		

Priority Applications (No Type Date): GB 8926960 A 19891129; GB 8926760 A 19891129
Cited Patents: NoSR.Pub; EP 143038; EP 2593631; EP 75651; FR 2593632
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 430487	A				
Designated States (Regional): DE FR IT NL					
US 5278086	A		8	H01L-027/105	
EP 430487	B1	E	10	G02F-001/136	
Designated States (Regional): DE FR IT NL					
DE 69019475	E			G02F-001/136	Based on patent EP 430487

GB 2238644 B G09G-003/18

Abstract (Basic): EP 430487 A

The matrix addressable display comprises a group of switchable cells (C11,C12,C21,C22) e.g. liquid crystal cells, having electrodes (3,5) on each of two parallel plates and thin-film drive transistors (T11,T12,T21,T22) disposed on one of the plates. **Gate** resistors (33,35) are provided by elongate doped polysilicon regions connecting the **gate** electrodes to address lines (23,25).

The **gate** resistors prevent short-circuiting of the address lines in the event of a **gate** short-circuit occurring in any of the transistors. (7pp Dwg.No.2/4)

Abstract (Equivalent): EP 430487 B

A method of forming a display of the kind comprising a group of switchable cells (C11, C12, C21, C22) disposed between first and second substantially parallel plates, each cell having a first electrode (3) on said first plate and a second electrode (5) on said second plate, in which each of a plurality of transistors (T11, T12, T21, T22) disposed on said first plate has two main electrodes and a **gate** electrode, and in which the main electrodes of each transistor are connected between a respective cell electrode on said first plate and a first address line (23,27), and the **gate** electrode of each transistor is coupled to a second address line (25, 23); the method comprising forming on said first plate a plurality of polysilicon channel regions (41, 43) for the transistors; insulating the channel regions; forming polysilicon **gate** regions (71, 73) for the transistors over the channel regions, together with a plurality of elongate polysilicon regions (69) of predetermined width to length ratio connected to the **gate** regions; doping at the same time the polysilicon **gate** regions, the channel regions where not **masked** by the **gate** regions, and the elongate polysilicon regions; said predetermined **width** to **length** ratio being such that when **doped** the elongate **regions** form **resistance** elements (49) whose **resistance** is sufficiently large to prevent address line short-circuiting; forming said second address line connected to the ends of the polysilicon resistance elements remote from the **gate** regions, and forming said first electrodes connected to said channel regions.

D23

Dwg.2/4

Abstract (Equivalent): GB 2238644 B

A method of forming a display of the kind comprising a group of switchable cells disposed between first and second substantially parallel plates, each cell having a first electrode on sad first plate and a second electrode on said second plate, in which each of a plurality of transistors disposed on said first plate has two main electrodes and a **gate** electrode, and in which the main electrodes of each transistor are connected between a respective cell electrode on said first plate and a first address line, and the **gate** electrode of each transistor is coupled to a second address line; the method comprising forming on said first plate a plurality of polysilicon channel regions for the transistors; insulating the channel regions; forming polysilicon **gate** regions for the transistors over the channel regions, together with a plurality of elongate polysilicon regions connected to the **gate** regions; doping the polysilicon **gate** regions, the channel regions where not **masked** by the **gate** regions, and the elongate polysilicon regions whereby said elongate regions form resistance elements; forming said second address line connected to the ends of the polysilicon resistance elements remote from the **gate** regions, and forming said first electrodes connected to said channel regions.

Abstract (Equivalent): US 5278086 A

Each cell has a first electride on the first plate and a second electrode on the second plate, in which each of a number of transistors disposed on the first plate has two main electrodes and a **gate** electrode. The main electrodes of each transistor are connected between a respective cell electrode on the first plate and a first address line. The **gate** electrode of each transistor is coupled to a second address line. On the first plate is formed a number of polysilicon channel regions, each channel region providing two of the transistors.

The channel regions are insulated and polysilicon **gate** regions formed for the transistors over the channel regions, together with elongate polysilicon regions connected to the **gate** regions. The polysilicon **gate** regions are doped, also the channel regions where not **masked** by the **gate** regions, and the elongate polysilicon regions. The elongate regions form resistance elements. The second address line connected to the ends of the polysilicon resistance elements is formed remote from the **gate** regions and the first electrodes are formed connected to the channel regions.

USE - For forming a display comprising a group of switchable cells disposed between two parallel plates.

Dwg.4e,f/4

Title Terms: MATRIX; ADDRESS; DISPLAY; FORMING; METHOD; RESISTANCE; ELEMENT ; TRANSISTOR; CIRCUIT; LIMIT; EFFECT; SHORT; CIRCUIT; OCCUR; TRANSISTOR
Derwent Class: P81; P85; U11; U12; U14
International Patent Class (Main): G02F-001/136; G09G-003/18; H01L-027/105
International Patent Class (Additional): G02F-001/13; G02F-001/1345; G09F-009/35; H01L-029/78
File Segment: EPI; EngPI
Manual Codes (EPI/S-X): U11-C18; U12-D02A; U14-H01A; U14-K01A2

12/9/9 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

004816370
WPI Acc No: 1986-319711/198649
XRPX Acc No: N86-238441

FET **for microwave applications - has reduced resistance zone between high resistance zones**

Patent Assignee: TECH HOCH LLMENAU (TEHO-N)
Inventor: SCHWIERZ F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DD 238134	A	19860806	DD 277021	A	19850605	198649	B

Priority Applications (No Type Date): DD 277021 A 19850605

Abstract (Basic): DD 238134 A

Between at least two zones of the active layer with a specified length related resistance at least one zone is arranged with reduced **length** related resistance. The reduced **length** related **resistance** is obtained by increasing the **doping** and/or increasing the cross **section** of the respective zone of the active layer.

USE/ADVANTAGE - Improvement of frequency limit and slope by exploiting overshoot effect is achieved using available technology. For micro-wave switching or amplification. (-pp Dwg.No.11/11

Title Terms: **FET** ; MICROWAVE; APPLY; REDUCE; RESISTANCE; ZONE; HIGH; RESISTANCE; ZONE

Derwent Class: U12
International Patent Class (Additional): H01L-029/80
File Segment: EPI
Manual Codes (EPI/S-X): U12-D02X

12/9/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004091993
WPI Acc No: 1984-237534/198438
XRAM Acc No: C84-100332
XRPX Acc No: N84-177735
Low resistance interconnection for integrated circuits - has polysilicon layer deposited over silicide, opt. with silicide free resistor regions
Patent Assignee: AADVANCED MICRO DEVICES INC (ADMI); ADVANCED MICRO DEVICES INC (ADMI)
Inventor: CHAN H W K
Number of Countries: 011 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8403587	A	19840913	WO 84US366	A	19840305	198438	B
EP 136350	A	19850410	EP 84901304	A	19840305	198515	
US 4569122	A	19860211	US 83473481	A	19830309	198609	

Priority Applications (No Type Date): US 83473481 A 19830309
Cited Patents: 5.Jnl.Ref; DE 3027954; DE 3131875; EP 29099; SSR871014; US 4214917; US 4329706; US 4364166; US 4389257; US 4392150; US 4403394; US 4419812; US 4443930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8403587	A	E	31		
Designated States (Regional): AT BE CH DE FR GB LU NL SE					
EP 136350	A	E			
Designated States (Regional): AT BE CH DE FR GB LI LU NL SE					

Abstract (Basic): US 4569122 A
In the mfr. of an integrated circuit with a low resistance quasi-buried contact between a polycrystalline layer and a heavily doped region of the substrate, a silicide layer is deposited over a region between the polycrystalline region and the substrate and extends to overlap these components. A polycrystalline Si layer is deposited over the silicide layer. A low resistance interconnection is provided between the polycrystalline layer and the substrate, regardless of the overlap distance between the polycrystalline layer and the substrate.
USE/ADVANTAGE - RAM cell mfr., in which additional **masking** steps are minimal and critical **mask** alignment is relieved.
(12pp
Abstract (Equivalent): WO 8403587 A
The interconnection is made to a first IC region by (a) depositing a silicide layer overlapping the first IC region; (b) depositing a polySi layer over the silicide; and (c) making a connection to the polySi at a second region to interconnect first and second regions. A load resistor may be incorporated in the structure by removing part of the silicide layer in a third region between first and second regions, and depositing polySi over first, second and third regions to define a polySi load resistor between the first and second regions. The inverted polycide sandwich is also used to provide a low resistance quasi-buried contact between two layers having a nominal interface region, where the silicide/polySi overlaps the interface region and adjacent portions of

the layers to provide low resistance contact between the layers, regardless of a possible lap of overlap between the layers.

ADVANTAGE - The inverted polySi structure may be incorporated in any standard **MOS** process to provide a second level of interconnect. The process requires min. additional **masking** steps, includes no critical **mask** alignments, and compensates for **mask** misalignment in forming quasi-buried contacts. The silicide layer reduces diffusion from highly **doped** substrate **regions** , and a desired effective **resistor length** may be achieved with smaller actual resistor length, reducing required area.

0/4

US 4569122 A

In the mfr. of an integrated circuit with a low resistance quasi-buried contact between a polycrystalline layer and a heavily doped region of the substrate, a silicide layer is deposited over a region between the polycrystalline region and the substrate and extends to overlap these components. A polycrystalline Si layer is deposited over the silicide layer. A low resistance interconnection is provided between the polycrystalline layer and the substrate, regardless of the overlap distance between the polycrystalline layer and the substrate.

USE/ADVANTAGE - RAM cell mfr., in which additional **masking** steps are minimal and critical **mask** alignment is relieved.

Title Terms: LOW; RESISTANCE; INTERCONNECT; INTEGRATE; CIRCUIT; POLY; SILICON; LAYER; DEPOSIT; SILICIDE; OPTION; SILICIDE; FREE; RESISTOR; REGION
Index Terms/Additional Words: INTEGRATE; CIRCUIT
Derwent Class: L03; U11; U13; U14
International Patent Class (Additional): H01L-021/74; H01L-023/48; H01L-029/46
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-D03D
Manual Codes (EPI/S-X): U11-C05C1; U11-C05C9; U13-D02; U14-A03B1

12/9/11 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04408354 **Image available**
DEVICE FOR GENERATING TRANSISTOR MODEL PARAMETER

PUB. NO.: 06-052254 [JP 6052254 A]
PUBLISHED: February 25, 1994 (19940225)
INVENTOR(s): MIYAHARA YASUTOKU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-201303 [JP 92201303]
FILED: July 28, 1992 (19920728)
INTL CLASS: [5] G06F-015/60; H01L-021/82
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.2 (ELECTRONICS -- Solid State Components)
JOURNAL: Section: P, Section No. 1746, Vol. 18, No. 287, Pg. 157, May 31, 1994 (19940531)

ABSTRACT

PURPOSE: To improve the accuracy of a circuit design by exactly generating a transistor model parameter of transistors of various shapes used for a circuit simulator.

CONSTITUTION: The shape information of a transistor to be derived is inputted in a transistor shaped input part 2. A model parameter of a reference transistor is stored in a reference transistor model parameter

storage part 3, and a joining **area** , depth of **doping** , sheet **resistance** , channel **width** , channel **length** , etc., are stored in a process and **mask** design data storage part 4, as process and **mask** design data of the reference transistor. When information of a transistor of a new shape is inputted, the difference to the new transistor is detected from the joining area, etc., of the reference transistor, and from this difference information, a new transistor model parameter is calculated by a new transistor model parameter calculating part 5.

12/9/12 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02692061 **Image available**
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 63-308961 [JP 63308961 A]
PUBLISHED: December 16, 1988 (19881216)
INVENTOR(s): IMAI KENJI
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-145692 [JP 87145692]
FILED: June 11, 1987 (19870611)
INTL CLASS: [4] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- **Metal Oxide Semiconductors** , **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 741, Vol. 13, No. 147, Pg. 153, April 11, 1989 (19890411)

ABSTRACT

PURPOSE: To improve arbitrariness and reproducibility of a **width** of a lightly **doped region** while reducing sheet **resistance** of a **gate** electrode without deteriorating finess of the structure, by providing a process for leaving a lightly doped region in alignment with oxidized side walls and a process for selectively depositing a tungsten film in place of a first layer.

CONSTITUTION: Dopant ions are implanted into a region directly under a **gate** oxide film 3 where a channel region is to be formed, so that a lightly doped region 4' is compensated thereby to have the same conductivity type to that of a substrate 1 and the threshold voltage is adjusted properly. In the final process, a residual first layer 5 of polycrystalline silicon having a reduced thickness in the **gate** region and oxide films 3', 3; are removed. A **gate** electrode 10 and contact electrodes 11s, 11d are selectively formed in the source and drain regions 9s and 9d from which the surface of single-crystal silicon is exposed. Another tungsten film is further superposed with the deposited tungsten film used as an initial film, so that the sheet resistance is reduced thereby. Thus, it is possible to improve arbitrariness and reproducibility of a width of the lightly doped region while reducing the sheet resistance of the **gate** electrode, without deteriorating finess of the structure.

12/9/13 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02373265 **Image available**

MANUFACTURE OF SEMICONDUCTOR ELEMENT

PUB. NO.: 62-290165 [JP 62290165 A]
PUBLISHED: December 17, 1987 (19871217)
INVENTOR(s): OKADA NORIAKI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-131694 [JP 86131694]
FILED: June 09, 1986 (19860609)
INTL CLASS: [4] H01L-027/04
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JOURNAL: Section: E, Section No. 615, Vol. 12, No. 187, Pg. 21, May 31, 1988 (19880531)

ABSTRACT

PURPOSE: To enable a high-resistance section to have a selectively decreased **thickness** , by forming polysilicon on a semiconductor substrate, **doping regions** thereof destined for low- **resistance sections** with an impurity, covering the polysilicon with non-oxidizing **mask** layers except a region destined for the high-resistance section, then oxidizing the region destined for the high-resistance section to a predetermined depth and finally removing the oxide film and the **mask** layers.

CONSTITUTION: A region of a polysilicon layer 13 destined for a high-resistance section 13a is oxidized to a predetermined depth. The oxide film 17 is then removed, whereby the thickness of the high-resistance section 13a is decreased. During said oxidation, regions of the polysilicon 13 destined for low-resistance sections 13b are not oxidized since they are covered with non-oxidizing **mask** layers 15 and 16. Accordingly, their thickness can be maintained at a predetermined level. On the other hand, the high-resistance section 13a is allowed to have a higher resistance value by decreasing its thickness. As a result, even if the high-resistance section 13a has a length as small as 4 .mu.m or less, decrease in resistance value caused by diffusion of impurities from the low-resistance section 13b to the high-resistance section 13a can be compensated and the resistance is maintained at a high level. When dimensions of the high-resistance section 13a are the same as those of conventional ones, a substantially higher resistance value can be obtained in comparison with the conventional ones.

12/9/14 (Item 1 from file: 95)

00708116 E93093309026

Compact GTO - a new gate **turn-off thyristor design for improved safe operating area**

(Kompakt-GTO: ein neuer Entwurf eines Abschalt- **Gate** -Thyristors fuer eine Sicherheitsverbesserung im Betriebsbereich)

Bakowski, M; Ljungberg, M; Elderstig, H; Norlin, P
Swed. Inst. of Microelectronics, Kista-Stockholm, S; Ellemtel Utvecklings AB, Aelvsjoe-Stockholm, S

ISPSD 92, IEEE 4th Int. Symp. on Power Semiconductor Devices and ICs, Proc., Tokyo, J, May 19-21, 19921992
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-7803-0813-1; 0-7803-0814-X

ABSTRACT:

A new **gate** turn-off thyristor (GTO) design is presented, where narrow cathode emitter-fingers (20-50 microm wide) are interdigitated with heavily **doped** p(+)- **regions** for low **resistance** **gate** -current transport. **Measurements** on fabricated 2 cm(exp 2) devices reveal excellent thyristor characteristics. The turn-off capability significantly better than that of the standard GTO devices with 200 microm wide emitters has been achieved with 5 times higher p-base lateral resistivity. At the same time up to 2 orders of magnitude reduction of minimum **gate** trigger current was achieved. It has been thus proven that it is possible to improve the trade-off between the turn-on and turn-off properties of GTO devices by the use of fine patterning.

DESCRIPTORS: THYRISTOR APPLICATIONS; POWER ELECTRONICS; **GATE** TURN OFF THYRISTORS; PERFORMANCE RELIABILITY; **GATE** -- **FIELD** **EFFECT** **TRANSISTOR** ; BREAKING CAPACITY; AMOUNT OF ELECTRIC RESISTANCE; COMPACT PACKAGE
IDENTIFIERS: GTO--(**GATE** TURN OFF THYRISTOR); Ausschaltthyristor; Betriebssicherheit
?

21/9/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012724098 **Image available**
WPI Acc No: 1999-530211/199945
XRAM Acc No: C99-156105
XRPX Acc No: N99-392999
Semiconductor device e.g. a short channel MOSFET
Patent Assignee: SIEMENS AG (SIEI)
Inventor: EISELE I
Number of Countries: 025 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 945905	A2	19990929	EP 99105957	A	19990324	199945	B
DE 19812945	A1	19990930	DE 1012945	A	19980324	199946	

Priority Applications (No Type Date): DE 1012945 A 19980324
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 945905	A2	G	13	H01L-029/78	
DE 19812945	A1			H01L-029/78	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Abstract (Basic): EP 945905 A2

NOVELTY - A semiconductor device, with a channel region (40) having different dopant concentration sections (74, 75) along its length between two different conductivity type doped regions (20, 30), is new.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (i) production of the above device by forming an electrode on a first conductivity type doped substrate, covering a region at one side of the electrode with a **mask** or a selectively oxidized **gate** oxide region, introducing first conductivity type dopant into an exposed region at the other side of the electrode to form a heavily doped section, removing the **mask** or oxidized **gate** oxide region and introducing second conductivity type dopant at both sides of the electrode to form a lightly doped section between two doped regions; and (ii) production of the above device by epitaxial growth on the substrate of a stack of a second doped region (30), the lightly doped (75) and heavily doped (74) sections of the channel (40) and a first doped region (20), followed by forming the **gate** oxide (65) and electrode (60) at the side of the stack.

USE - E.g. as a short channel **MOSFET** .

ADVANTAGE - The device exhibits a minimal Ron value because of its reduced channel **length** , increased breakdown **resistance** because of the electric field reduction due to the lightly **doped** channel **section** , reduced channel **resistance** because of the increased mobility due to the lightly **doped** channel **section** and independent variation of the Ron value and the turn-on voltage UT.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic view of an n-channel **MOSFET** according to the invention.

Substrate (10)
First and second doped regions (20, 30)
Channel region (40)
Gate electrode (60)
Gate oxide (65)
Heavily doped channel section (74)
Lightly doped channel section (75)
pp; 13 DwgNo 3/6

Title Terms: SEMICONDUCTOR; DEVICE; SHORT; CHANNEL; **MOSFET**

Derwent Class: L03; U12
International Patent Class (Main): H01L-029/78
International Patent Class (Additional): H01L-021/336; H01L-029/10
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02; L04-E01B1
Manual Codes (EPI/S-X): U12-D02A

21/9/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003331866
WPI Acc No: 1982-H9879E/198227
Low voltage integrated MOS transistor protection - has greatly increased impurity concentration in base of lateral bipolar transistor for lower breakdown voltage
Patent Assignee: SGS ATES COMPONENTI ELTRN SPA (SGSA); SGS-ATES COMP

ELETT (SGSA)
Inventor: BALDI L
Number of Countries: 006 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
FR 2494501	A	19820521				198227 B
GB 2090701	A	19820714	GB 8134626	A	19811117	198228
NL 8105192	A	19820616				198228
DE 3145592	A	19820715				198229
JP 57112076	A	19820712				198233
GB 2090701	B	19840926				198439
IT 1150062	B	19861210				198842
NL 189789	B	19930216	NL 815192	A	19811116	199309
DE 3145592	C2	19930429	DE 3145592	A	19811117	199317

Priority Applications (No Type Date): IT 8026063 A 19801119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2494501	A		17		
NL 189789	B		10	H01L-029/78	
DE 3145592	C2		8	H01L-027/06	

Abstract (Basic): FR 2494501 A

The **MOS** integrated circuit requires input protection to prevent its destruction during normal handling. This protection may be afforded to an IGFET in which **gate** isolation oxide is less than 500 Angstroms by a lateral bipolar transistor. The emitter and collector regions are doped with the same type and density of impurity as the source and drain regions of the IGFET.

The emitter is earthed and the collector connected to the input **gate** . The base region of the transistor is doped with a much higher impurity concentration than the other regions of the same type in the circuit. This is achieved by adding two stages, a **masking** and an ion implantation to the standard PLANOX (RTM) process. The **size** and **doping** of the base **region** are adjusted such that the breakdown and negative **resistance** phenomena in the transistor are manifest at a voltage lower than the insulating oxide of the **gates** and the bipolar junctions of the transistors in the integrated circuit will break down at, and so that the sustaining voltage of the transistor is greater than the supply voltage.

4

Abstract (Equivalent): GB 2090701 B

An **MOS** integrated circuit of low supply voltage and high integration density, comprising a first signal input terminal, a second terminal for connection to earth, a third terminal for connection to a power supply, at least one IGFET transistor with **gate** insulation oxide having a thickness not greater than 500 angstroms, and a protection device against input over-voltages comprising a lateral bipolar transistor with emitter and collector regions doped with the same type and same concentration of impurities as the source and drain regions of the IGFET transistor, the emitter region being electrically connected to the earth terminal and the collector region being electrically connected to the input terminal and to the **gate** electrode of the IGFET transistor, the impurity concentration in the base region of the lateral transistor being much higher than in the other regions of the same polarity of the integrated circuit, the extension of the base region and the concentration of impurities therein being such as to provide the breakdown voltage and the triggering voltage of negative resistance phenomena of the lateral transistor at a value lower than the breakdown voltage of the **gate** insulating oxide and lower than the breakdown voltage of bipolar junctions included in the integrated circuit, and such as to provide the sustaining voltage of the lateral transistor at a value higher than the integrated circuit supply voltage.

Title Terms: LOW; VOLTAGE; INTEGRATE; **MOS** ; TRANSISTOR; PROTECT; INCREASE; IMPURE; CONCENTRATE; BASE; LATERAL; BIPOLAR; TRANSISTOR; LOWER; BREAKDOWN ; VOLTAGE

Index Terms/Additional Words: METAL; OXIDE; SEMICONDUCTOR

Derwent Class: U12; U13; U24

International Patent Class (Main): H01L-027/06; H01L-029/78

International Patent Class (Additional): H01L-023/56; H01L-023/58; H02H-007/20; H02H-009/04; H03F-001/00

File Segment: EPI

Manual Codes (EPI/S-X): U12-D02A; U13-D02; U24-X

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Set     Items   Description
S1   14186712   WIDTH OR BREADTH OR THICKNESS OR SIZE OR SIZES OR MEASUREM-
             ENT? OR DIMENSION?
S2    3091810   RESISTOR OR RESISTANCE
S3     886178   GATE?
S4     420908   MASK?
S5    4505384   MOS? ? OR MOSFET? ? OR FET? ? OR METAL()OXIDE()SEMICONDUCT-
             OR? OR FIELD()EFFECT?()TRANSIST? OR PMOS OR CMOS
S6     789425   DOPED OR DOPING OR DOPE
S7   12265838   REGION? OR SECTION? OR SEGMENT? OR AREA?
S8      30971   S6(6N)S7
S9       1530   (S1 OR LENGTH?) AND S2 AND S8
S10        43   (S1 OR LENGTH?) (3N) S2 (3N)S8
S11        21   S10 AND (S3 OR S4 OR S5)
S12        14   RD (unique items)
S13        86   S9 AND S3 AND S4 AND S5
S14        85   S13 NOT S12
S15        85   RD (unique items)
S16         1   S15 AND PD<=20030804
S17        82   S15 AND PY<=2003
S18       111   (S1 OR LENGTH?) (6N) S2 (6N)S8
S19         3   S18 AND S3 AND S4 AND S5
S20         3   S19 NOT S16
S21         2   S20 NOT S12
S22      6865   S3(3N)S4
S23      4210   S3(2N)S4
S24      2584   S23 AND (S5 OR TRANSISTOR?)
S25   4007298   ORIFICE? OR VENT? ? OR OUTLET OR OUT()LET? OR APERTURE? OR
             HOLE? ?  OR OPENING? OR CUT()OUT OR CUTOUT?
S26       404   S24 AND S25
S27       124   S1 AND S26
S28        23   S2 AND S27
S29        23   RD (unique items)
S30        23   S29 NOT (S12 OR S21)
? show files
File   2:INSPEC 1969-2004/Jul W2
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Jul W3
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Jul W2
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W2
         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
File  94:JICST-EPlus 1985-2004/Jun W4
         (c)2004 Japan Science and Tech Corp(JST)
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File 144:Pascal 1973-2004/Jul W2
         (c) 2004 INIST/CNRS
File 647:CMP  Computer Fulltext 1988-2004/Jul W2
         (c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Jul 20
         (c) 2004 The Dialog Corp.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jul W3
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01109408 CMP ACCESSION NUMBER: EET19961104S0054

FET process shows path to high-speed circuits

Gail Robinson

ELECTRONIC ENGINEERING TIMES, 1996, n 926, PG41
PUBLICATION DATE: 961104
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Technology
WORD COUNT: 1217

TEXT:

Santa Barbara, Calif. - A new process for building compound semiconductor **field - effect transistors** , developed here by researchers at the University of California, may offer a route to ultra-dense gallium-arsenide and indium-phosphide circuits. Called super self- aligned submicron single metal **FET** (SASSFET), the technology offers a simpler option for reaching 0.2-micron design rules using conventional optical lithography, according to researchers on the project.

The technology is claimed to be independent of the material system or the kind of device used. It can be implemented for any **FET** process and is considered to be less expensive and easier to work with than current standard technologies. Initial work has produced a 0.4-micron -gate-length junction-modulated heterostructure **FET** (JHFET) based on InGaAs, with a 45-GHz short-circuit current-gain cutoff frequency and an 80-GHz maximum frequency of oscillation.

"We had two goals in mind when working toward this concept," said Primit Parikh, a researcher in the Department of Electrical and Computer Engineering. "We wanted to make self-aligned devices that could not be made using e-beam lithography and to use simple optical photolithography techniques to get down to submicron device features. "

Parikh pointed out that a wide application base exists for very fast **FETs** , regardless of the material system used. "You can do a 0.2 device, let's say a HEMT, by e-beam technology that will have the same speed, but this method would offer a cheaper and easier way to do it," Parikh said.

In addition to its self-aligned gate technique, the process features a one-step process for creating source, gate and drain contacts. In fact, those structures can be formed simultaneously with the interconnect metal, leading to a single-metal-level design, according to Parikh.

An additional advantage is that the technology can be used in dense circuits for the integration of n- **FETs** with heterostructure bipolar **transistors** -a combination that can provide high frequency with the load-driving ability of bipolar **transistors** .

The project has successfully tested the merged-device concept by integrating an n-junction **FET** and a pnp HBT in which the p gate represents the emitter of the HBT. As a result, a highly integrated device combination creates an n- **FET** in the lateral direction and a pnp HBT in the vertical direction.

The basic design reason for using a self-aligned process was to develop a high-performance **FET** with a low knee voltage. "If you don't make a self-aligned device, you will get an access **resistance** between the source and gate region," explained Parikh. "With a self- aligned device, the gate region is right next to the source; therefore there is no access region. The result is a low access **resistance** , due to the fact that it is so close."

The proximity of source and drain is particularly important for low-mobility material systems.

The key to the self-alignment is the introduction of a dummy gate made of a dielectric such as silicon dioxide or silicon nitride. The dummy gate plays the role of a conventional gate in the first steps of the process and is then removed. At a later stage, the real gate is formed in a "T" geometry in such a way that it automatically aligns itself with previously defined features.

The basic approach does not depend on any particular material system. "Right now, when you need a self-aligned device, it does not necessarily have to be the same material system as GaAs," said Parikh.

By using metal/organic chemical-vapor deposition (MOCVD) to define contact, the researchers were able to apply self-aligned techniques for defining the source and drain contacts. The standard for source and drain are gold germanium contacts that are alloyed to the channel , but those cannot withstand temperatures of 450 degrees C or 500 degrees C. Using MOCVD, the researchers regrew the source and drain region and then added tungsten, a temperature-stable metal, for the contact.

"The regrown contacts give you the option of using high-temperature steps in your process to gain other benefits in device definition," said Parikh.

An important cost advantage is that the system is based on single-metal technology. Typically, in **FET** fabrication, there are two metallization steps:one for the gate and one for the source and drain. But when the material for the source and drain is regrown with SASSFET technology, the gate and the source/drain can be done in a single step, thus directly reducing cost by eliminating steps.

During processing, the first step places the dummy gate with standard optical lithography, for which the smallest **dimension** is 1 micron. That step is followed by etching down to the channel region. Because the source-drain is right next to the gate, a sidewall is built that separates the source and the gate by a small amount-about 2,000A or 0.2 micron. Thus, the sidewall eliminates the possibility of a short.

Next, selective regrowth is done using MOCVD, based on the fact that oxide or nitride prevents regrowth. The result is that no material grows on the gate region and the sidewall region, but it does grow everywhere else on the wafer.

The sidewall that defined the spacing between the gate and the source and drain is then removed by plasma etching, and the silicon dioxide or silicon nitride are replaced by a metal.

For planarization purposes, poly-dimethyl-glutar-imide, a photoresist made by Microlithography Corp. that is sensitive to deep- UV, is spun over the device. It is then removed until the top of the dummy gate is exposed, thus protecting everything except the top of the gate. When put in the hydrofluoric acid, the silicon dioxide or silicon nitride is etched away, leaving a **hole** for the gate.

The researchers went with a T-gate contact for the actual metal gate, because they defined the initial area with a 1.0-micron **gate mask** and then shrunk it to 0.4 micron. "The T structure was important because as you go to lower gate lengths, the gate **resistance** becomes significant," Parikh said. "So, if you have a wider top and a narrower bottom, you can get faster and faster devices without putting up the **resistance** ."

The T-gate geometry is key to getting smaller devices from a relatively relaxed optical-lithography capability. "For optical lithography, you can get 1.0 micron easily, then keep shrinking it until it goes down to 0.4 micron," said Parikh.

For prototyping purposes, the current process used two metal steps. When the actual gate metal is placed, the source and drain metal can also be defined.

"It just means defining one more metal layer," said Parikh. "We could have easily combined the two steps, but we did not have the right mask during our original work."

While there are several challenges in using the technique, such as exact control of the equipment, Parikh believes that in a manufacturing environment precise control will not be an issue.

For example, in depositing the dummy gate using nitride it is necessary that exactly the same amount be used every time. And because the next step is to shrink the geometry with plasma etching, the exact etch rate is critical. Such requirements can be difficult in a university environment but could be more readily addressed with dedicated manufacturing equipment.

The research team is working toward 0.2- and 0.1-micron devices and also plans to get the technology up to faster speeds. The current goal is to build 450-GHz **FETs** .

30/9/2 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00588890 CMP ACCESSION NUMBER: EET19910304S1778
CAREER OPPORTUNITIES IN SOFTWARE - Software picture firms up
GEORGE ROSTKY
ELECTRONIC ENGINEERING TIMES, 1991, n 631, 72
PUBLICATION DATE: 910304
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Profession: Work Week
WORD COUNT: 1179
TEXT:

Major software companies are hiring, but not at the frenetic pace of the past. There are soft spots, but the major companies do have **openings** .

One of these is Mentor Graphics, of Beaverton-no, make that Wilsonville, Ore. The largest outfit in electronic-design-automation software, Mentor is moving from the many buildings it's been leasing in Beaverton to a spanking new campus it owns in Wilsonville, a dozen miles to the south. The move should be completed within a month.

Mentor is best known for its software, which covers the spectrum from front-end tools to back-end CAD tools, including mechanical packaging and integrated documentation. **Most** of the software has been operating on systems from Hewlett-Packard's Apollo Systems Division. This year, Mentor will extend its operations to platforms from Sun Microsystems and others.

The company employs 2,475 people, 1,200 in Oregon. Though **most** of its engineering is centered in Wilsonville, it also has an IC product group and a board-product group in San Jose, Calif., where there are 275 people. There are additional design centers in Salt Lake City and in Warren, N.J., thanks to the acquisition in May of Silicon Compiler Systems Corp.

Mentor has 600 software engineers in the United States and it's looking for 35 more. Dick Anderson, vice president for human resources , would like engineers with strength in ASICs, standard ICs, pc boards and, across the board, analog circuitry. Though he expects to hire 35 engineers this year, he does not expect the head count to grow.

The new hires are expected, mainly, to compensate for normal attrition. "Overall," says Anderson, "relative to years when we might have added 100 engineers or more, this year will see a sharp reduction."

Despite Mentor's move, Beaverton hasn't emptied out. Logic Automation Inc., located there, writes software models to emulate hardware components, mainly standard logic chips and microprocessors. The company boasts a library of 10,000 devices. Says Jim Higgs, director of human resources: "We're growing nicely."

The company has 110 employees, about half of them engineers, most of them on the software side. The software people develop the tools, of course, but Logic Automation hires quite a few hardware people, says Higgs, because they are so familiar with the various hardware components. "We teach them how to write software," he says. "Lots of engineers learn both hardware and software these days. The separation isn't as clear as it was in the past. You don't find a hardware engineer these days who doesn't know how to do some programming."

Higgs plans to hire more than 25 engineers this year, mostly software people. "It would be great," he says, "if we could find engineers familiar with modeling and even greater if we could find people familiar with various CAE tools." Higgs expects to do limited college hiring and intends to hire engineers with BS or MS degrees and experience ranging from zero to substantial.

He expects a healthy growth rate of 50 to 75 percent this year. That's not as brisk as last year's growth, when the company essentially doubled.

Down south, way past Wilsonville, Ready Systems (Sunnyvale, Calif.) creates development tools for real-time embedded systems. Ready has 160 people, including 70 software engineers in several locations, 30 of them in Sunnyvale.

It is seeking five engineers in Sunnyvale at two levels of experience: three to five years and five and above. In each case, Dave Gremer, director of engineering, would like degrees in EE or CS, preferably at the master's level, and experience in Unix, C and embedded real-time systems.

Salaries are in the range of $55K to $65K for the senior position, $40K to $55K for the other.

Still further south, Quadratron Systems Inc. (Westlake Village, Calif.) makes office-automation software, mostly on DOS and Unix operating systems. The software covers such functions as word processing, electronic mail, spreadsheets, calendars and personal filing.

The company employs 50 people, including a dozen engineers. Larry Lipstone, director of software development, wants to add about two engineers with some X Window experience. "There isn't a great deal of X Window experience out there," he says, "so we feel it's OK to breed our own internally." He's also looking for DOS programmers who can integrate DOS into a Unix environment. And he'd like a good programmer in Unix and C.

Salaries, he says, can go to the $50s, "maybe higher if we find somebody super." Lipstone would prefer engineers with degrees, but that's not mandatory. "We don&APOSTRon

While QuickLogic disclosed only its design tools, it also provided some information about its forthcoming "user-programmable ASIC" (pASIC) hardware.

For starters, the chip will be a dense, field-programmable gate-array-like device with about the same equivalent gate figures as competitive FPGAs, said president and chief executive officer David Laws. He rated the initial chips at between 1,000 and 4,000 equivalent gates, based on the **size** of an equivalent **mask** -programmed **gate** array. This is the measure used by Actel for rating its devices, and it is considerably more conservative than the raw-gate figures used by Xilinx and Altera.

Like the Xilinx devices, the QuickLogic arrays will be matrices of relatively small logic cells. The schematic symbols on the QuickLogic software indicate that each cell will contain a small number of gates connected to a single flip-flop. It appears that the cells are optimized for synchronous design methodologies, with emphasis on J-K and clock inputs, rather than on asynchronous inputs.

Seemingly, the greatest innovation in the QuickLogic parts is in the company's proprietary interconnect scheme. Laws distinguished the new

technique from techniques based on memory technology, such as Xilinx's SRAM switches or conventional EPLD EPROM cells. He also claimed that the technology was different from that used in the Actel antifuse.

Laws said that while other FPGA vendors must accept interconnect impedances in the range of 1k to 10k ohms, the QuickLogic technology would have much lower **resistance** , and thus would enjoy a significant speed advantage. He claimed that the company has 4-bit counters running at 106 MHz in sample devices.

In addition, QuickLogic tool developers said the new interconnect scheme is much simpler and more orthogonal than that used in Xilinx arrays, where routing tools must choose between three types of interconnect.

One apparent disadvantage of the new technology also emerged at the disclosure. The device requires a programming algorithm so unique that it apparently isn't easy to implement on existing programmers. This is one reason QuickLogic gave for including its own programmer in its development kit. But the company is confident that commercial programmers would quickly adapt to the new chip's requirements.

The overall picture is of a medium-scale FPGA with a relatively fine structure and fast, easily routed interconnects. The density of the parts will make them a viable alternative to devices ranging from Altera's Max family to at least the middle of the Xilinx line, and their speed should make them the only alternative for very fast-more than 50-MHz-designs..END {MS {FM {BT

30/9/3 (Item 1 from file: 350)

014686319 **Image available**
WPI Acc No: 2002-507023/200254
XRAM Acc No: C02-144066
XRPX Acc No: N02-401190

Semiconductor device manufacturing method involves forming threshold implant by implanting impurities into substrate, using silicon nitride layer and side wall spacer as mask

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: HUSTER C R; ISHIDA E; MILIC-STRKALJ O
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6395606	B1	20020528	US 99357918	A	19990721	200254	B

Priority Applications (No Type Date): US 99357918 A 19990721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6395606	B1		8	H01L-021/336	

Abstract (Basic): US 6395606 B1

NOVELTY - Ion impurities are implanted into main surface (200a) of semiconductor substrates (200) through an **opening** to form a threshold implant, using a silicon nitride layer and side wall spacers (220), formed above substrate as **mask** . **Gate** oxide layer (201) is formed in exposed portion of substrate not covered by the spacers. A doped polysilicon layer (202) is formed on the gate oxide and the spacers.

DETAILED DESCRIPTION - Metal layers (203) are formed to fill the **opening** .

USE - For forming semiconductor devices such as **metal oxide semiconductor field effect transistor** (**MOSFET**).

ADVANTAGE - Parasitic junction capacitance is reduced by blocking the threshold implant from the source/drain region. The gate **resistance** is decreased and the switching speed of the device is increased.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor device.

Semiconductor substrate (200)
Main surface (200a)
Gate oxide layer (201)
Doped polysilicon layer (202)
Metal layer (203)
Spacers (220)
pp; 8 DwgNo 2/2

Technology Focus:

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Method: A spacer formation layer of silicon dioxide is deposited to a **thickness** of about 100 Angstrom in the **opening** . The spacer formation layer is anisotropically etched to form the sidewall spacers extending to the exposed portion of the substrate about 100 Angstrom or less. The gate oxide layer is grown to a **thickness** of 20 Angstrom and a polysilicon layer is deposited to a **thickness** of 150 Angstrom-200 Angstrom on the gate oxide and the side wall spacers. The ion impurities are implanted to form the doped polysilicon layer and tungsten is deposited to form a metal layer. The ion impurities are implanted into the substrate to form a lightly or moderately doped source/drain implant. A threshold implant is formed by implanting impurities such as boron or arsenic at an energy of about 2 KeV to 5 KeV and at a dosage of about 4 x 10 to the power 15 atoms per cm squared, using the spacers and the silicon nitride as mask. The threshold implant and the source/drain implants are electrically activated by heating. The metal layer covering the doped polysilicon layer is planarized to expose the silicon nitride layer and portions of the doped polysilicon layer. A protective silicon dioxide layer is thermally grown on the exposed portions of the polysilicon layer.

Title Terms: SEMICONDUCTOR; DEVICE; MANUFACTURE; METHOD; FORMING; THRESHOLD ; IMPLANT; IMPLANT; IMPURE; SUBSTRATE; SILICON; NITRIDE; LAYER; SIDE; WALL; SPACE; MASK
Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-021/336
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02B; L04-C10; L04-C10B; L04-C12A; L04-C12B
Manual Codes (EPI/S-X): U11-C02B2; U11-C02J6; U11-C04D; U11-D03C3A; U12-D02A

30/9/4 (Item 2 from file: 350)

013972374 **Image available**
WPI Acc No: 2001-456587/200149
XRAM Acc No: C01-138016
XRPX Acc No: N01-338345

Production of self-aligned contact used in, e.g. flash memory cells, involves forming metal silicide on polysilicon gate and diffusion regions, and forming self-aligned contact etch mask **on the** gates **and sidewall spacers portion**

Patent Assignee: ALLIANCE SEMICONDUCTOR CORP (ALLI-N)
Inventor: SHRIVASTAVA R
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6258714	B1	20010710	US 99283727	A	19990401	200149	B

Priority Applications (No Type Date): US 99283727 A 19990401

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6258714	B1		9	H01L-021/8234	

Abstract (Basic): US 6258714 B1

NOVELTY - A self-aligned contact is made by forming a metal silicide on a polysilicon gate and diffusion regions; forming a self-aligned contact etch mask over the silicided polysilicon gate and to sidewall spacers portion; forming an interlayer dielectric layer; and depositing a contact interconnect material in a contact **hole** created by the self-aligned contact etch.

DETAILED DESCRIPTION - Production of self-aligned contact involves providing a semiconductor substrate (202) having diffusion regions (208); and forming a polysilicon gate (206) having sidewall spacers (210) on the substrate. The polysilicon gate is separated from the substrate by a gate oxide (204). A metal silicide (224, 225) is then formed on the polysilicon gate and the diffusion regions. A self-aligned contact etch mask (230) is then formed over the silicided gate (222) and to the sidewall spacers portion. The mask has contact **hole** in a portion of diffusion regions. An interlayer dielectric layer is then formed over the **masked gate** and silicided diffusion regions. A self-aligned contact etch of the interlayer dielectric is conducted, and a contact interconnect material is deposited in a contact **hole** created by the self-aligned contact etch.

USE - The method is used for forming self-aligned contacts in silicided **metal oxide semiconductor** (**MOS**) devices (200), such flash memory cells, dynamic random access memory (DRAM), or static random access memory (SRAM).

ADVANTAGE - The method provides self-aligned contact and improved reliability and decreased **resistance** to the **MOS** devices.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of self-aligned contact.

MOS devices (200)
Substrate (202)
Gate oxide (204)
Polysilicon gate (206)
Diffusion regions (208)
Sidewall spacers (210)
Silicided gate (222)
Metal silicide (224, 225)
Etch mask (230)
pp; 9 DwgNo 2F/3

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: Isolation regions and gate dielectric layer are formed on a substrate prior to formation of polysilicon gate. A second polysilicon gate is also provided on the substrate, such that the contact is formed between the two polysilicon gates. The interlayer dielectric layer is subjected to chemical-mechanical polishing prior to self-aligned contact etching. A tungsten plug is formed in the contact **hole** .

Preferred Condition: The metal is converted to silicide by heating at not more than 1000 degreesC.

Preferred **Dimension** : The semiconductor device is at **most** 0.25 microns. The etch stop mask overlaps the sidewall spacers by 20-50% of the device's gate **width** , or 0.1 microns.

INORGANIC CHEMISTRY - Preferred Material: The metal silicide comprises titanium silicide or cobalt silicide. The self-aligned contact etch stop mask comprises silicon oxynitride or silicon nitride. The contact interconnect material comprises polysilicon, aluminum, aluminum copper, or tungsten. The metal used to form metal silicide comprises titanium, cobalt, or titanium/titanium nitride

Title Terms: PRODUCE; SELF; ALIGN; CONTACT; FLASH; MEMORY; CELL; FORMING; METAL; SILICIDE; GATE; DIFFUSION; REGION; FORMING; SELF; ALIGN; CONTACT; ETCH; MASK; GATE; SIDEWALL; SPACE; PORTION
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/8234
International Patent Class (Additional): H01L-021/4763
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C07; L04-C10; L04-C10B; L04-C11C; L04-C12A; L04-C13A; L04-C13B
Manual Codes (EPI/S-X): U11-C05B7; U11-C05D3; U11-C05E1; U11-C05G2C; U11-C07; U11-D03B2

30/9/5 (Item 3 from file: 350)

013846702 **Image available**
WPI Acc No: 2001-330915/200135
XRAM Acc No: C01-101840
XRPX Acc No: N01-238292

Gate electrode formation for e.g. field effect transistor - **involves using resist mask with** aperture **having** width **larger than** apertures **on insulating films, for etching cap layer on which gate electrode is deposited**

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11354538	A	19991224	JP 98159073	A	19980608	200135	B

Priority Applications (No Type Date): JP 98159073 A 19980608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11354538	A		5	H01L-021/338	

Abstract (Basic): JP 11354538 A

NOVELTY - An **aperture** (103h) is formed on an insulating film (103) by isotropic etching via **aperture** (104h) on insulating film (104) used as mask. The **width** of **aperture** (103h) is larger than the **width** of **aperture** (104h). Then, a resist mask (107) with **aperture** (107h) of larger **width** is used for etching cap layer (102) on which gate electrode (108) is deposited.

DETAILED DESCRIPTION - The cap layer and the insulating films (103,104) are sequentially formed over the semiconductor substrate (100).

USE - For semiconductor device e.g. **field effect transistor** .

ADVANTAGE - Reduces stray capacitance between gate electrode and semiconductor substrate thereby reducing source **resistance** .

DESCRIPTION OF DRAWING(S) - The figure is the cross sectional view explaining the gate electrode formation process. (100) Semiconductor substrate; (102) Cap layer; (103,104) Insulating films; (103h,104h) **Apertures** ; (107) Resist **mask** ; (108) **Gate** electrode.

Dwg.1/2

Title Terms: GATE; ELECTRODE; FORMATION; FIELD; EFFECT; **TRANSISTOR** ; RESIST; MASK; **APERTURE** ; **WIDTH** ; LARGER; **APERTURE** ; INSULATE; FILM; ETCH; CAP; LAYER; GATE; ELECTRODE; DEPOSIT
Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-021/338
International Patent Class (Additional): H01L-029/812
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C06C; L04-C11C; L04-E01A
Manual Codes (EPI/S-X): U11-C18A3; U12-D02B

30/9/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595494 **Image available**
WPI Acc No: 2001-079701/200109
XRAM Acc No: C01-022846
XRPX Acc No: N01-060659
Manufacture of semiconductor device involves ion implantation of impurities into the substrates through the oxide layer and at the exposed portions of the main surface to form the source and drain regions
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: BESSER P R; KEPLER N; WANG L; WIECZOREK K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6162689	A	20001219	US 98187231	A	19981106	200109	B

Priority Applications (No Type Date): US 98187231 A 19981106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6162689	A		12	H01L-021/336	

Abstract (Basic): US 6162689 A

NOVELTY - A semiconductor device is made by ion implantation of impurities into the substrates (300) through the oxide layer and at the exposed portions of the main surface to form source and drain regions (340). The metal layer is formed on the regions, and heated to form a metal silicide layer.

DETAILED DESCRIPTION - Manufacture of a semiconductor device involves forming conductive gates on a main surface of a semiconductor substrate. The spacers are formed on side surfaces of the gates. An oxide layer is formed on the main surface, spacers, and **gates** . A **mask** is formed on the oxide layer. It has **openings** spaced apart from the spacers. The **openings** correspond to portions of the main surface where the silicided contacts are to be formed. The oxide layer is exposed to portions of the main surface. The impurities are ion implanted into the substrate through the oxide layer and at the exposed portions of the main surface to form the source and drain regions having a first junction depth below the oxide layer and having a second junction depth, greater than the first junction depth, below the exposed portions of the main surface where the silicided contacts are to be formed. A metal layer is formed on the source and drain regions and heated to form a metal silicide layer. The second junction depth is below the metal silicide layer.

USE - For manufacturing semiconductor device having silicided source/drain regions, particularly high-density semiconductor devices of at **most** 0.18 mum.

ADVANTAGE - The invention enables formation of shallow source and

drain regions having ultra-shallow junctions of high integrity with cobalt silicide contacts of optimized **thickness** . It enables the formation of cobalt silicide layers with improved electrical characteristics, and facilitates device scaling by enabling the formation of low- **resistance** silicided source/drain regions having ultra-shallow junctions without silicided-related junction leakage.

DESCRIPTION OF DRAWING(S) - The figure schematically illustrates sequential phases of the invented method.

Substrates (300)
Gates (315)
Spacers (325)
Source and drain regions (340)
pp; 12 DwgNo 3E/4

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method includes heating at a first temperature to form a first-phase metal silicide layer and rapid thermal annealing at 400-550degreesC (preferably 470degreesC); and heating at a second temperature to form a second-phase metal silicide layer having a resistivity lower than that of the first-phase metal silicide layer, and includes rapid thermal annealing at 700-900degreesC (preferably 825degreesC). The metal layer is formed on the oxide layer; and etched to remove the metal layer from the oxide layer after forming the first-phase metal silicide layer. The oxide layer is formed by plasma enhanced chemical vapor deposition (PECVD) and by thermal oxidation. The gates (315) are formed by forming a polysilicon layer on the main surface; forming a tungsten silicide layer on the polysilicon layer; forming a mask over portions of the tungsten silicide layer corresponding to the gates; and etching unmasked portions of the tungsten silicide layer and the polysilicon. Impurities are ion implanted into the substrate near the gates to form lightly doped implants prior to forming the spacers (325).

INORGANIC CHEMISTRY - Preferred Layers: The metal layer comprises cobalt, the first-phase metal silicide layer comprises cobalt silicide (CoSi) and the second-phase metal silicide layer comprises cobalt silicide (CoSi2).

Preferred Properties: The oxide layer has a **thickness** of 20-500 Angstrom. The polysilicon layer is formed with a **thickness** of 1500-2500 Angstrom (preferably 2000 Angstrom). The tungsten silicide layer has a **thickness** of 200-800 Angstrom (preferably 400). The polysilicon layer has an impurity concentration of at least 1x1019 cm-3. The lightly doped implants have a junction depth of 500-1500 Angstrom. The first junction depth is 1000-1700 Angstrom, and the second junction depth is 1500-2000. The formed mask is spaced apart from the spacers at 500-2000 Angstrom (preferably 1000 Angstrom).

Title Terms: MANUFACTURE; SEMICONDUCTOR; DEVICE; ION; IMPLANT; IMPURE; SUBSTRATE; THROUGH; OXIDE; LAYER; EXPOSE; PORTION; MAIN; SURFACE; FORM; SOURCE; DRAIN; REGION

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/336

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C02B; L04-C10F; L04-C11

Manual Codes (EPI/S-X): U11-C02B2; U11-C02J6; U11-C05F1; U11-C18A3

30/9/7 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010084892 **Image available**

WPI Acc No: 1994-352605/199444

Related WPI Acc No: 1994-327732; 1994-352783; 1994-352784; 1995-189135

XRAM Acc No: C94-160547
XRPX Acc No: N94-276842
Thin film transistor mfr. with improved prodn. yield - by laser irradiation of impurity doped domain through layer insulation film before formation of source and drain electrodes
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: KONUMA T; KOYAMA I; MIYAZAKI M; MURAKAMI A; SUGAWARA A; TAKEMURA Y; UEHARA Y; UOCHI H; ZHANG H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6275641	A	19940930	JP 9386752	A	19930322	199444 B
KR 166397	B1	19990115	KR 945917	A	19940322	200037

Priority Applications (No Type Date): JP 9386752 A 19930322; JP 9386750 A 19930322; JP 9386751 A 19930322; JP 93263024 A 19930927
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6275641	A		4	H01L-021/336	
KR 166397	B1			H01L-029/78	

Abstract (Basic): JP 6275641 A
The **transistor** is formed on a substrate (11) over which ground insulation film (12) is formed . An island like polycrystal semiconductor domain (13) is formed on the insulation film. A gate insulation film (14) and gate electrode (15) of aluminium with anodising layer (16) are formed. The impurity doping of the semiconductor layer is carried out to form source and drain impurity domains (17a,17b) using **gate** electrode as **mask** . The laser irradiation of the impurity domains is carried out after the formation of contact **holes** (19a,19b), then source and drain electrodes of titanium nitride/aluminium (20) are formed.
ADVANTAGE - Reduces contact **resistance** of impurity domain. Improves prodn. yield of thin film **transistor** . Minimises variation of characteristics.
Dwg.1/2
Abstract (Equivalent): US 5580800 A
A method of forming a **transistor** comprising:
forming an aluminum film having a **thickness** of 2000 to 10000 Angstrom and containing a Group IIIb element of the Periodic Table;
patterning the aluminum film by etching; and
removing a residue comprising the Group IIIb element produced by the patterning step.
(Dwg.10/12
Title Terms: THIN; FILM; **TRANSISTOR** ; MANUFACTURE; IMPROVE; PRODUCE; YIELD ; LASER; IRRADIATE; IMPURE; DOPE; DOMAIN; THROUGH; LAYER; INSULATE; FILM; FORMATION; SOURCE; DRAIN; ELECTRODE
Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-021/336; H01L-029/78
International Patent Class (Additional): H01L-029/784
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02D; L04-C10B; L04-C11C; L04-C12B; L04-C13A
Manual Codes (EPI/S-X): U11-C18A1

30/9/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009980692 **Image available**

WPI Acc No: 1994-248406/199430
XRAM Acc No: C94-113571
XRPX Acc No: N94-197210
Prodn. of self aligned cobalt silicide T-gate for silicon@ MOS devices - includes forming masking oxide layer on polysilicon layer over gate oxide layer, depositing cobalt on mask heating to react cobalt layer with polysilicon layer in mask opening over gate etc.
Patent Assignee: ALLIED-SIGNAL INC (ALLC)
Inventor: CAVIGLIA A L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5334545	A	19940802	US 9311632	A	19930201	199430	B

Priority Applications (No Type Date): US 9311632 A 19930201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5334545	A		4	H01L-021/283	

Abstract (Basic): US 5334545 A
process for making a self-aligned cobalt silicide T-gate for silicon **MOS** devices comprises forming gate oxide layer on a top surface of a silicon substrate; forming a polysilicon layer on the gate oxide layer; forming a masking oxide layer on the polysilicon layer, the masking oxide layer having an **opening** exposing a gate region on the polysilicon layer. A layer of cobalt is deposited on the masking oxide layer and the gate region of the polysilicon layer; followed by heating the substrate to react the cobalt layer with said polysilicon layer in said **opening** to form a cobalt silicide layer in the gate region, the cobalt layer deposited on the masking oxide layer remaining unreacted. The unreacted portion of the cobalt layer and masking oxide layer are removed to expose the polysilicon layer in the region not covered by cobalt silicide layer; and the exposed polysilicon layer is removed using the cobalt silicide as a mask to form the self-aligned cobalt silicide T-gate.
ADVANTAGE - Lower gate **resistance** and a significant redn. in polysilicon layer **thickness** is obtd. giving easier planarisation layers and easier etching of sub-micron gates.
Dwg.4/4
Title Terms: PRODUCE; SELF; ALIGN; COBALT; SILICIDE; GATE; SILICON; **MOS** ; DEVICE; FORMING; MASK; OXIDE; LAYER; POLY; SILICON; LAYER; GATE; OXIDE; LAYER; DEPOSIT; COBALT; MASK; HEAT; REACT; COBALT; LAYER; POLY; SILICON; LAYER; MASK; OPEN; GATE
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/283
International Patent Class (Additional): H01L-021/336
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C10B; L04-C10F
Manual Codes (EPI/S-X): U11-C05D4; U11-C05E2; U11-C05E3; U11-C05F1

30/9/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008885701 **Image available**
WPI Acc No: 1992-012970/199202
XRAM Acc No: C92-133963
XRPX Acc No: N92-230076
Junction FET mfr. on SOI - includes using focussed ion beam technique

for gate electrode formation
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: INOUE Y; MORIMOTO H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3263332	A	19911122	JP 9063034	A	19900313	199202	B
US 5141880	A	19920825	US 91669080	A	19910312	199237	

Priority Applications (No Type Date): JP 9063034 A 19900313
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 3263332	A		5		
US 5141880	A		19	H01L-021/265	

Abstract (Basic): JP 3263332 A
A JFET mfg. method comprises (a) implanting a first conducting type impurity into a monocrystalline silicon layer to be used as an active layer on an insulating layer; (b) covering the layer surfaces with a silicon oxide film; (c) implanting a second conducting type impurity into the gate electrode-forming portion of the silicon layer by a focussed ion beam method; (d) implanting metal ions into the gate electrode-forming portion of the silicon oxide film by a focussed ion beam method; (e) forming an impurity-doped polysilicon gate electrode over an area larger than the gate electrode-forming portion of the silicon oxide film; and (f) implanting a second conductivity type impurity into the silicon layer, using the polysilicon **gate** electron as **mask** , to form source and drain regions.
ADVANTAGE - Use of the focussed ion beam technique allows formation of a gate electrode and channel region with 0.1 micron diameter at the buried portion and 0.1 micron **width** so that, even if the channel impurity concn. is increased to 1x10 power 17/cm.cm for reduced **resistance** , the channel region can be fully depleted by reverse bias voltage application and thus the drain current can be controlled. The gate electrode can be formed without special lithography and etching of an **aperture** in the silicon layer and the silicon oxide film, and device planarity is improved. (First major country equivalent to J03263332)
Title Terms: JUNCTION; **FET** ; MANUFACTURE; SOI; FOCUS; ION; BEAM; TECHNIQUE ; GATE; ELECTRODE; FORMATION
Derwent Class: L03; U11; U12
International Patent Class (Main): H01L-021/265
International Patent Class (Additional): H01L-021/33; H01L-029/80
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L04-C02B; L04-C11C; L04-C12A; L04-E01A1
Manual Codes (EPI/S-X): U11-C02J6; U11-C05E1; U12-D02B; U11-C08A6; U11-C18A3
Derwent Registry Numbers: 1694-U

30/9/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007571093
WPI Acc No: 1988-205025/198829
XRAM Acc No: C88-091544
XRPX Acc No: N88-156477
Metal-strapped polysilicon gate electrode for FET device - provides a planar low sheet resistance **device without causing intermixing of dual**

work function dopants

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: ABERNATHEY J R; CRONIN J E; LASKY J B
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4755478	A	19880705	US 8784719	A	19870813	198829 B
EP 303061	A	19890215	EP 88111163	A	19880712	198907
JP 1133368	A	19890525	JP 88137585	A	19880606	198927
EP 303061	B1	19920527	EP 88111163	A	19880712	199222
DE 3871457	G	19920702	DE 3871457	A	19880712	199228
			EP 88111163	A	19880712	

Priority Applications (No Type Date): US 8784719 A 19870813
Cited Patents: 3.Jnl.Ref; A3...8917; EP 106458; EP 68897; No-Sr.Pub; US 3994758; US 4453306
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4755478	A		8		
EP 303061	A	E			
	Designated States (Regional): DE FR GB				
EP 303061	B1	E	13	H01L-021/28	
	Designated States (Regional): DE FR GB				
DE 3871457	G			H01L-021/28	Based on patent EP 303061

Abstract (Basic): US 4755478 A

A metal-strapped polysilicon gate **FET** is mfd. by:- 1. Defining a gate stack on an exposed surface of a semiconductor substrate, the gate stack including a **gate mask** disposed on a patterned polysilicon layer, 2. Defining first and second diffusion regions in the substrate having first and second silicide electrodes disposed thereon to form source and drain electrodes. 3. Depositing an insulating layer on the substrate and planarising it to expose an upper surface of the **gate mask** . 4. Removing the **gate mask** to define an **aperture** in the insulating layer that exposes the polysilicon layer. 5. Depositing a low sheet **resistance** conductive material on the substrate to fill, at least partially, the **aperture** in the industry layer to provide a gate electrode that is relatively co-planar with the planarised insulating layer.

USE/ADVANTAGE - In the mfr. of highly dense semiconductor memory devices. Provision of a planarised, low sheet **resistance FET** device without causing intermixing of duol work function dopants.

0/6

Abstract (Equivalent): EP 303061 B

A process of forming a planarised, metal-strapped polysilicon gate **FET** , comprising the steps of: defining a gate stack on an exposed surface of a semiconductor substrate, said gate stack including a gas mask disposed on top of a patterned polysilicon layer; defining first and second diffusion regions in said substrate having first and second silicide electrodes formed thereon by refractory metal deposition and subsequent annealing, said first and second diffusion regions being self-aligned to said gate stack and forming source and drain electrodes of said **FET** , said **gate mask** preventing silicide formation over said polysilicon layer; depositing an insulating layer on said substrate,, said insulating layer having a **thickness** substantially equal to that of said gate stack; planarising said insulating layer so as to expose an upper surface of said **gate mask** ; removing said **gate mask** to define an **aperture** in said insulating layer that exposes said polysilicon layer; and depositing a low sheet **resistance** conductive material on said substrate to at least partially fill said

aperture in said insulating layer so as to form a gate electrode of said **FET** that is relatively co-planar with said planarised insulating layer.

Title Terms: METAL; STRAP; POLY; SILICON; GATE; ELECTRODE; **FET** ; DEVICE; PLANE; LOW; SHEET; **RESISTANCE** ; DEVICE; CAUSE; INTERMIXING; DUAL; WORK; FUNCTION; DOPE
Derwent Class: L03; U11; U13
International Patent Class (Main): H01L-021/28
International Patent Class (Additional): H01L-021/42; H01L-021/90; H01L-029/78
File Segment: CPI; EPI
Manual Codes (CPI/A-N): L03-G04A; L04-C11C; L04-E01A
Manual Codes (EPI/S-X): U11-C05E; U11-C05F1; U11-C18A; U13-D02A

30/9/11 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007309094
WPI Acc No: 1987-306101/198743
XRPX Acc No: N87-228781
Field effect transistor **with high gain and output power at 18 ghz - has channel doped to give maximum transconductance and minimise source** resistance **and has heavily doped semiconductor substrate**
Patent Assignee: GOULD INC (GOUN)
Inventor: KAKIHANA S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4698899	A	19871013	US 86835706	A	19860303	198743	B

Priority Applications (No Type Date): US 83543479 A 19831019; US 86835706 A 19860303; US 86835707 A 19860303
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4698899	A		7		

Abstract (Basic): US 4698899 A
The **field effect transistor** (**FET**) has a channel region which is heavily doped under the gate and between the gate and the source of the **FET** . The channel region between the gate and the drain is lightly doped and the **FET** is formed on a heavily doped semiconductor substrate. The method of making the **FET** comprises providing a mask layer over a lightly doped channel region and forming **openings** in the mask layer such that a portion of the mask is located at the gate location and has a predetermined **width** and height.
Ion implanting is performed at a predetermined angle such that a portion of the channel adjacent the source is heavily doped and a second portion of the channel adjacent the drain is not exposed due to the height of the **mask** at the **gate** .
ADVANTAGE - High output breakdown voltage.
4/8
Title Terms: FIELD; EFFECT; **TRANSISTOR** ; HIGH; GAIN; OUTPUT; POWER; GHZ; CHANNEL; DOPE; MAXIMUM; TRANSCONDUCTANCE; MINIMISE; SOURCE; **RESISTANCE** ; HEAVY; DOPE; SEMICONDUCTOR; SUBSTRATE
Derwent Class: U11; U12
International Patent Class (Additional): H01L-021/42
File Segment: EPI
Manual Codes (EPI/S-X): U11-C02J6; U12-D02X

30/9/12 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004371220
WPI Acc No: 1985-198098/198533
XRAM Acc No: C85-086468
XRPX Acc No: N85-148665

ROM having small size memory cell with low drain contact resistance - has drain electrode extending over two insulating films over gate electrode, and wiring layer over drain electrode

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: ARIIZUMI S; IWASE T; MASUOKA F

Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 151476	A	19850814	EP 85101074	A	19850201	198533	B
JP 60163455	A	19850826	JP 8417782	A	19840203	198540	
US 4748492	A	19880531	US 8721573	A	19870303	198824	
EP 151476	B	19900516				199020	
DE 3577781	G	19900621				199026	

Priority Applications (No Type Date): JP 8417782 A 19840203
Cited Patents: 1.Jnl.Ref; A3...8643; DE 2909996; EP 54163; EP 68897; JP 58027359; No-SR.Pub; US 4372031
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 151476	A	E	15		
Designated States (Regional): DE FR GB					
EP 151476	B				
Designated States (Regional): DE FR GB					

Abstract (Basic): EP 151476 A

A ROM comprises (a) source and drain regions formed in a semiconductor substrate; and (b) a gate electrode formed on an insulating film over the substrate between source and drain regions; (c) a drain electrode contacting the drain regions with low contact **resistance** and partly covering second and third insulating films formed over the gate electrode; and (d) a wiring layer on the drain electrode.

The device is mfd. by (i) forming a gate electrode on a insulating film on the substrate; (ii) forming source and drain regions in the substrate using the **gate** electrode as **mask** ; (iii) forming second and third insulating films covering the gate electrode and having a common contact **hole** exposing the drain region; (iv) forming a drain electrode extending through the **hole** to contact the drain region and extending above the gate electrode; and (v) forming a metal wiring layer on the drain electrode.

ADVANTAGE - The **size** of the memory cell is reduced, e.g. 15% smaller than a cell made by the conventional field oxide method. Contact **resistance** between the cell and the output line is low, avoiding degradation of **transistor** characteristics.

1/5

Abstract (Equivalent): EP 151476 B

A read only memory comprising: a semiconductor substrate (11); a source region (13) and a drain region (12) both formed in said substrate; a gate electrode (1) formed on a first insulating film (21) formed on an area of said substrate (11) which is between said source

region (13) and said drain region (12); a drain electrode (14) contacting said drain region (12) and consisting of a material so as to provide a low contact **resistance** therebetween, the drain electrode extending onto an insulation layer (22,23) formed on said gate electrode (1); and a metal wiring layer (2) formed on a further insulating layer (24) and contacting said drain electrode (14), characterised in that: said insulation layer comprises second and third insulating films (22,23); said drain electrode (14) partially covers the gate electrode (1); and said wiring layer (2) contacts a portion of said drain electrode (14), said portion including and extending beyond a contact portion of said drain electrode (14) with said drain region (12). (10pp)

Abstract (Equivalent): US 4748492 A

Read only memory has two **MOS** **transistors** with separate sources and a common drain. Gate insulation films for each **transistor** are on the substrate and gate electrodes are on the gate insulation films. Insulation films are on each electrode and further insulation films define a contact **hole** to the common drain. A common drain electrode in the contact **hole** contacts the drain and has an extending portion on the second insulation film above each gate electrode. Another insulation film is on the extended portion above the gate electrodes and defines a second contact **hole** above the first one. A conductive layer is on the common drain electrode and insulation film, and extends into the second contact **hole** and contacting the drain electrode.

USE/ADVANTAGE - **MOSFET** ROM mfr. in which contact between the memory cell and output line is minimised. (9pp)

Title Terms: ROM; **SIZE** ; MEMORY; CELL; LOW; DRAIN; CONTACT; **RESISTANCE** ; DRAIN; ELECTRODE; EXTEND; TWO; INSULATE; FILM; GATE; ELECTRODE; WIRE; LAYER; DRAIN; ELECTRODE

Index Terms/Additional Words: **READ-ONLY** ; **MEMORY**

Derwent Class: L03; U11; U12; U14

International Patent Class (Additional): G11C-017/00; H01L-021/82; H01L-023/48; H01L-027/10; H01L-029/54

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-D04; L03-G04

Manual Codes (EPI/S-X): U11-C05C4; U12-D02A; U12-E02; U14-A06B

30/9/13 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

06564798 **Image available**

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 2000-150541 [JP 2000150541 A]

PUBLISHED: May 30, 2000 (20000530)

INVENTOR(s): FUJIMOTO HIROMASA
UDA TOMOYA
OTA TOSHIMICHI
MASATO HIROYUKI
MATSUNO TOSHINOBU

APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD

APPL. NO.: 11-356203 [JP 99356203]
Division of 07-212289 [JP 95212289]

FILED: August 22, 1995 (19950822)

PRIORITY: 06-196606 [JP 94196606], JP (Japan), August 22, 1994 (19940822)
07-063971 [JP 9563971], JP (Japan), March 23, 1995 (19950323)

INTL CLASS: H01L-021/338; H01L-029/812; H01L-021/265; H01L-021/28

ABSTRACT

PROBLEM TO BE SOLVED: To provide a manufacturing method for forming a high-performance power GaAS MESFET with an improved yield while highly maintaining a gate/drain breakdown voltage.

SOLUTION: A WSi film 71a is deposited on a GaAs substrate 70, and an Si ion is implanted using a mask 72, to form an active layer 74a. Then, by using a mask 73 with a narrow **opening** , a B ion is injected with a weak acceleration voltage to form a high- **resistance** layer 75 wide than a gate formation region. Further, by using a mask 78 with a narrower **opening** , an Mg ion is implanted to form a p-type region 90 in the high- **resistance** layer 75. A metal film 76 on a gate made of Au is formed at the **opening** of the mask 78 by the lift-off method, a WSi film 71a is subjected to patterning with the metal film 76 on the **gate** as a **mask** , and a **gate** electrode 71 made of WSi is formed right above the p-type region 90. An **FET** with a high degree of freedom for design can be obtained by arbitrarily changing the **width** and depth of an i-layer (the high- **resistance** layer 75).

30/9/14 (Item 2 from file: 347)

DIALOG(R)File 347:JAPIO

04433581 **Image available**

THIN-FILM SEMICONDUCTOR DEVICE

PUB. NO.: 06-077481 [JP 6077481 A]
PUBLISHED: March 18, 1994 (19940318)
INVENTOR(s): YOSHIHASHI HIDEO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-228577 [JP 92228577]
FILED: August 27, 1992 (19920827)
INTL CLASS: [5] H01L-029/784; G02F-001/133; G02F-001/1343; G02F-001/136
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 29.2 (PRECISION INSTRUMENTS -- Optical Equipment)
JAPIO KEYWORD:R011 (LIQUID CRYSTALS); R097 (ELECTRONIC MATERIALS -- **Metal Oxide Semiconductors** , **MOS**)
JOURNAL: Section: E, Section No. 1565, Vol. 18, No. 326, Pg. 85, June 21, 1994 (19940621)

ABSTRACT

PURPOSE: To eliminate that a crack and a flaw are caused in an interconnection part by a method wherein a gate electrode is formed as a two-layer structure composed of a lower-layer polycrystalline silicon thin film and of an upper-layer thin-film metal silicide and the line **width** and the sheet **resistance** of the gate electrode are set respectively at specific values or lower.

CONSTITUTION: A polycrystalline silicon thin film 2 is formed on an insulating substrate 1. It is worked to be an island shape, and a silicon oxide film 3 is formed on its surface. Then, a polycrystalline silicon film 4 is formed, it is then doped with impurities such as phosphorus or the like, and an activation heat treatment is executed to lower its **resistance** . In succession, a metal silicide film 5 is formed, the polycrystalline silicon film and the metal silicide film in parts other than essential

parts such as a gate interconnection part and the like are removed, and the line **width** of a gate electrode is set at 20.mu.m. After that, a heat treatment is executed, the gate part its set at 15cm/ square or lower, impurities are implanted by a self-alignment method using the **gate** as a **mask** , and a source diffused region 6 and a drain diffused region 7 are formed. Then, a silicon oxide film 8 is formed, and a contact **hole** in a source-drain part is formed. An aluminum film 9 is deposited, inessential parts are removed, a heat treatment is executed and an interconnection is completed.

30/9/15 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03581235 **Image available**
MANUFACTURE OF **MOS TRANSISTOR**

PUB. NO.: 03-244135 [JP 3244135 A]
PUBLISHED: October 30, 1991 (19911030)
INVENTOR(s): HONDA TAKESHI
APPLICANT(s): NEW JAPAN RADIO CO LTD [326320] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-039676 [JP 9039676]
FILED: February 22, 1990 (19900222)
INTL CLASS: [5] H01L-021/336; H01L-029/784
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- **Metal Oxide Semiconductors** , **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 1159, Vol. 16, No. 31, Pg. 128, January 27, 1992 (19920127)

ABSTRACT

PURPOSE: To provide a **MOS transistor** by implanting ions into a source region with a polysilicon **gate** as a **mask** , thermally diffusing the ions to form a lightly doped tub, carrying out ion implantation with a CVD film applied to the side wall of a gate, and forming source and drain regions through annealing.

CONSTITUTION: Field oxide 2, gate oxide 3, and a polysilicon gate 4 are formed on a P(sup -) silicon substrate 1. After a photoresist mask is applied to the substrate, ions are implanted into a source region and thermally diffused sideways to form an n(sup -) tub 5. A CVD film is formed to provide a side spacer 6, and there are formed a p(sup +) drain 7a, a p(sup +) source 7b, and an n(sup +) source contact layer 8 by ion implantation through an **opening** and heat treatment. Then, a CVD oxide film 6, aluminum interconnections, and a protective film 11 are provided. Since the edges of the implanted layer fall short by the **width** of the spacer 6 in this structure, greater room for diffusion of source and drain is provided so that the **resistance** to punchthrough is ensured easily.

30/9/16 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02723029 **Image available**
COMPOUND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 01-020629 [JP 1020629 A]

PUBLISHED: January 24, 1989 (19890124)
INVENTOR(s): TANAKA YUUJI
KANAMORI MIKIO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-177396 [JP 87177396]
FILED: July 16, 1987 (19870716)
INTL CLASS: [4] H01L-021/318; H01L-021/316; H01L-029/80
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals)
JOURNAL: Section: E, Section No. 756, Vol. 13, No. 198, Pg. 119, May 11, 1989 (19890511)

ABSTRACT

PURPOSE: To freely adjust a threshold voltage and to improve the nondefective rate of products by laminating a plurality of layers each having two types of reverse internal stresses in the formation of an insulating film on an insulating substrate on which elements including a **FET** are integrated, and reducing the film **thickness** on a **FET** element.

CONSTITUTION: Interlayer insulating films 7-9 each having two types of compression and tension stresses are laminated under a predetermined condition on a semi-insulating GaAs substrate 1 on which elements, such as a **resistor** operation layer 2, a **FET** operation layer 3 and a diode operation layer 4 and the like are integrated. Accordingly, when with resist as a **mask** on the **gate** electrode 5 of a **FET** it is opened and a **measurement** of a threshold voltage and an etching back of an interlayer insulating film of the **opening** due to RIE are repeated, the value of the threshold of the **FET** can be finely adjusted. As a result, the nondefective rate of products is enhanced.

30/9/17 (Item 5 from file: 347)

02266279 **Image available**
MANUFACTURE OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 62-183179 [JP 62183179 A]
PUBLISHED: August 11, 1987 (19870811)
INVENTOR(s): OGISHIMA JUNJI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-023726 [JP 8623726]
FILED: February 07, 1986 (19860207)
INTL CLASS: [4] H01L-029/78; H01L-029/54
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- **Metal Oxide Semiconductors**, **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 577, Vol. 12, No. 26, Pg. 33, January 26, 1988 (19880126)

ABSTRACT

PURPOSE: To improve the quality of a gate insulating film by gettering the pollutant of photoresist film removing a conductive layer and the gate insulating film at the conductive layer by a method wherein a connecting **hole** for direct contact is formed by removing a part of conductive layer forming a gate electrode on the gate insulating film of a MISFET as well as the gate insulating film.

CONSTITUTION: Impurity (e.g., phosphorus) to reduce **resistance** value is led to a gate insulating film 4 and a field insulating film 2 to form a polycrystalline silicon film 5a in **thickness** almost making gettering feasible before the pollutant (e.g., Na(sup +)) from a photoresist film for etching **mask** reaches the **gate** insulating film 4. Next, an etching mask 11 (photoresist film) with a part of source region or drain region opened is formed on a film 5a to remove the film 5a and the film 4 successively by etching process using this mask 1 and then a connecting **hole** 4A (for direct contact) exposing a semiconductor substrate 1 is formed. Through the connecting **hole** 4A formed in the gate insulating film 4, an interconnection 5B is connected to be composed of the same conductive layer as that of a gate electrode 4A of other MISFET adjoining the interconnection 5B.

30/9/18 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02197376 **Image available**
MANUFACTURE OF SEMICONDUCTOR ELEMENT

PUB. NO.: 62-114276 [JP 62114276 A]
PUBLISHED: May 26, 1987 (19870526)
INVENTOR(s): TAKAHASHI SEIICHI
ITO MASAAKI
KIMURA KENICHI
UENISHI KATSUZO
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-253651 [JP 85253651]
FILED: November 14, 1985 (19851114)
INTL CLASS: [4] H01L-029/80; H01L-021/28
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals); R100 (ELECTRONIC MATERIALS -- Ion Implantation)
JOURNAL: Section: E, Section No. 551, Vol. 11, No. 325, Pg. 107, October 22, 1987 (19871022)

ABSTRACT

PURPOSE: To reduce a gate **resistance** without increasing the **thickness** of a gate metal film by selectively growing W by means for reacting gas containing W with Si formed on a gate electrode forming portion to form a gate electrode.

CONSTITUTION: The channel layer 2 of **FET** is formed by implanting impurity ions into a GaAs semi-insulating substrate 1, an insulating film 3 is formed, with a resist 4 as a **mask** the **gate** forming portion of the film 3 is etched to form a **hole** 5. A polysilicon 6 is formed in the **hole** 5, the polysilicon 6 is re placed with a W metal film 7 by utilizing the reaction of WF(sub 6) with Si, H(sub 2) gas having reduction of WF(sub 6) gas is, for example, fed to seed the film 7, thereby forming the W metal film also on part on the film 3. After the film 3 is re moved, with the film 7 as mask for ion implanting to ion implant and anneal a contacting layer 8, thereby forming an ohmic metal layer 9 on the layer 8.

30/9/19 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

02032975 **Image available**
MANUFACTURE OF SCHOTTKY BARRIER GATE TYPE **FIELD EFFECT TRANSISTOR**

PUB. NO.: 61-247075 [JP 61247075 A]
PUBLISHED: November 04, 1986 (19861104)
INVENTOR(s): HIRAKATA NOBUYUKI
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-087942 [JP 8587942]
FILED: April 24, 1985 (19850424)
INTL CLASS: [4] H01L-029/80
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals); R100 (ELECTRONIC MATERIALS -- Ion Implantation)
JOURNAL: Section: E, Section No. 492, Vol. 11, No. 95, Pg. 106, March 25, 1987 (19870325)

ABSTRACT

PURPOSE: To obtain an MESFET in which source and drain electrodes are approached to a gate electrode as near as possible by forming an operating layer on the surface of a semiconductor substrate, then selectively ion implanting to reduce a source **resistance** , and forming a recess of an active layer and electrodes for the implanted layer in a self-aligning manner.

CONSTITUTION: An N-type conductive type epitaxial layer 13 and a mask 14 are formed on a high **resistance** buffer layer 12 on a semi-insulating substrate 11. A light implanted layer 15 is formed by ion implanting, an ohmic metal 16 is formed by sputtering, and source and drain electrodes 17, 18 are formed by etching back the entire surface. With the electrodes as masks the layer 13 is etched through a **hole** 19, and a recess 20 is formed to form the operating layer of an MESFET in a suitable **thickness** . Further, with the electrodes 17, 18 as **masks** a **gate** metal is deposited, and a gate electrode 21 is formed in the recess 20. In this case, a gate metal 21' to be deposited on the electrodes 17, 18 gradually reduces the **hole** 19 by a tangential law. Thus, the shape of the electrode 21 is gradually narrowed toward an upward direction to form the shape for hardly shortcircuiting the electrodes 17, 18.

30/9/20 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01797962 **Image available**
MANUFACTURE OF SOLID-STATE IMAGE PICKUP DEVICE

PUB. NO.: 61-012062 [JP 61012062 A]
PUBLISHED: January 20, 1986 (19860120)
INVENTOR(s): NISHIZAWA JUNICHI
TANAKA AKIMASA
APPLICANT(s): RES DEV CORP OF JAPAN [330319] (A Japanese Company or Corporation), JP (Japan)
NISHIZAWA JUNICHI [000000] (An Individual), JP (Japan)
TANAKA AKIMASA [000000] (An Individual), JP (Japan)
APPL. NO.: 59-131154 [JP 84131154]
FILED: June 27, 1984 (19840627)
INTL CLASS: [4] H01L-027/14; H04N-005/335
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 44.6

(COMMUNICATION -- Television)
JAPIO KEYWORD:R100 (ELECTRONIC MATERIALS -- Ion Implantation); R132 (ELECTRONIC MATERIALS -- Electrostatic Induction Type **Transistors** , SIT)
JOURNAL: Section: E, Section No. 409, Vol. 10, No. 158, Pg. 21, June 06, 1986 (19860606)

ABSTRACT

PURPOSE: To obtain a high-sensitivity solid-state image pickup device having no dispersion of **dimension** and sensitivity characteristic among the picture elements and having the flatly formed light-receiving surface, an excellent absorption efficiency of light and uniform characteristics by a method wherein a tunnel injection structure is adopted for the formation of the source region and the gate and source regions are formed by the diffusion conducted only once and a thermal treatment to be performed after that.

CONSTITUTION: A buried layer 2 is formed in the programming region for forming a **transistor** on an Si substrate 1, a high- **resistance** Si epitaxial growing layer 3 is formed thereon and a field oxide film 7 is further formed. Then, **apertures** are provided according to the first **mask** alignment process, **gate** insulating films 14 are formed there, an **aperture** is provided in the programming region for forming a **transistor** for photoelectric conversion according to the second mask alignment process, a tunnel injection oxide film 5 is formed there, and moreover, a conductive layer 8 is formed on the whole surface. Then, **apertures** are provided in the programming region for forming the gate of the **transistor** for photoelectric conversion and the programming regions for forming the source and drain of a **transistor** for scanning circuit according to the third mask-alignment process, an ion-implantation is performed in the regions, wherein the **apertures** are provided, and after an insulating film is formed on the whole surface, the ion implanted layers are activated.

30/9/21 (Item 9 from file: 347)

01477375 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 59-188975 [JP 59188975 A]
PUBLISHED: October 26, 1984 (19841026)
INVENTOR(s): IWAMATSU SEIICHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-063264 [JP 8363264]
FILED: April 11, 1983 (19830411)
INTL CLASS: [3] H01L-029/78; H01L-029/62
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- **Metal Oxide Semiconductors** , **MOS**); R100 (ELECTRONIC MATERIALS -- Ion Implantation
JOURNAL: Section: E, Section No. 300, Vol. 09, No. 49, Pg. 33, March 02, 1985 (19850302)

ABSTRACT

PURPOSE: To keep high the melting point of a gate electrode and improve the productivity as a low **resistance** by a method wherein the gate electrode of the **MOS** semiconductor device is made of Ti, and the source and drain are formed by self-alignment type with the Ti **gate** as a **mask** .

CONSTITUTION: A field oxide film 2 is formed on the surface of an Si wafer 1 by thermal oxidation, **holes** are bored in the oxide film 2 and the regions serving as the source, drain, and gate by photoetching method. Next, a gate oxide film 3 is formed by thermal oxidation, and a Ti film 4 is formed to a fixed **thickness** by the thermal decomposition of Ti chloride by pressure reduction CVD method, thus forming the Ti gate electrode 4 by photoetching. Then, the source region 5 and the drain 6 are formed by self-alignment type by ion implantation with the electrode 4 as a mask, and then the junction region therebetween is activated by means of lamp annealing. Then, the melting point of the gate electrode is kept high and made low resistant, resulting in the improvement of the productivity.

30/9/22 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

01241171 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 58-178571 [JP 58178571 A]
PUBLISHED: October 19, 1983 (19831019)
INVENTOR(s): KATSUKAWA KIMIAKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-061888 [JP 8261888]
FILED: April 14, 1982 (19820414)
INTL CLASS: [3] H01L-029/80; H01L-021/302
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R044 (CHEMISTRY -- Photosensitive Resins)
JOURNAL: Section: E, Section No. 222, Vol. 08, No. 13, Pg. 145, January 20, 1984 (19840120)

ABSTRACT

PURPOSE: To obtain an **FET** for low noise and high gain ultrahigh frequency by superposing an insulating film which has a **hole** by deciding a length of one direction of a Schottky barrier electrode on an insulating film which has a **hole** by deciding a length of one direction of a recess on the surface of a low **resistance** semiconductor layer.

CONSTITUTION: Insulating layers 31, 32 of different etching performance are laminated on a semiconductor layer 30, and a resist mask 33 is covered. It is sequentially selectively etched and opened with a window, the film 31 is etched at the side face, thereby forming an optimum recess **width** . Then, the layer 30 is etched in the optimum depth, a gate metal 34 is covered, a photoresist 33 used as a **mask** on the **gate** , and unnecessary gate metal is removed. A substrate recess is sufficiently cleaned, the surface contaminant is baked out, and the gate metal is then covered. According to the structure, an **FET** in which preferable Schottky junction can be formed, the gate length is not widened, the gate capacity is small, the gate withstand strength is high, the internal **resistance** is low with high gain and high reliability can be formed.

30/9/23 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

01106174 **Image available**
FIELD EFFECT TRANSISTOR

PUB. NO.: 58-043574 [JP 58043574 A]
PUBLISHED: March 14, 1983 (19830314)
INVENTOR(s): TSUKAGOSHI TSUNEO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-141744 [JP 81141744]
FILED: September 10, 1981 (19810910)
INTL CLASS: [3] H01L-029/78
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- **Metal Oxide Semiconductors**, **MOS**)
JOURNAL: Section: E, Section No. 179, Vol. 07, No. 129, Pg. 18, June 04, 1983 (19830604)

ABSTRACT

PURPOSE: To prevent the reduction of film **thickness** of a gate electrode and obtain a **field effect transistor** with a good manufacturing yield by performing a source diffusion with this insulating **gate** as a **mask**, by foring a struture wherein an Si nitride film is superposed on a gate electrode on a gate insulting film.

CONSTITUTION: The lamination of a gate oxide film 4, an As doped low **resistance** gate poly Si 5 and a nitride film 6 respectively in a fixed **thickness** is applied to a patterning by a photo resist film 7 resulting in the formation of an **aperture** part 8. Next, the nitride film 6, poly Si 5 and the gate oxide film 4 are successively etched by a reactive ion etching with this resist **aperture** part as a mask. Subsequently, boron is implanted as a base impurity, and a thin nitride film 10 is formed on the surface of the **aperture** part of the substrate 1, after the resist film 7 is removed. Next, a source region 3 is formed by implanting P as a source impurity with the insulating **gate** as a **mask**. Thereat, the P is implanted onto the surface of the base region 2 through the thin Si nitride film 10 but trapped into the thick nitride film in places other than it.
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